The First China RISC-V Forum

November 12-13

Lecture Hall, 3F, CII Building, Tsinghua Shenzhen International Graduate School, University Town, Nanshan District, Shenzhen•China

RISC-V is growing up very fast in China these years, and the open source silicon development ecosystem is getting more and more improved. It shows up at the emerging areas such as IoT, AI, Self-driving, edge computing and makes a lot of innovation and changes from computer architecture ISA to system SW. It is a clear trend that microprocessor design and development based the open source ISA becomes more and more important in IT industry.

In the 2019 China RISC-V forum (https://crvf2019.github.io/index_en.htm), we want to identify the challenges in building an open and free ecosystem of RISC-V, and pay special attention to the industrial and academic efforts, innovations and projects on RISC-V in China, including but not limited to FPGA and IC based chip design (both high performance and low-power), compiler and system software support, design tool flow, domain specific design and application, and so on.

We invite practitioners, academicians, and researchers who are passionate about advancing RISC-V ecosystem to join us. **Register Link：** https://www.wjx.top/jq/46235372.aspx

Forum Organizers：

- RIOS (RISC-V International Open Source Research Labs) and TBSI (Tsinghua-Berkeley Shen Zhen Research Institute)
- RISC-V Foundation China Committee
- CRVA (China RISC-V Alliance) and ICT (Institute of Computing Technology) at CAS (Chinese Academy of Sciences)

Organizing Committee

- **General Chair:**

  Zhangxi Tan

  Tsinghua-Berkeley Shen Zhen Research Institute　Adjunct Professor

  RISC-V International Open Source Research Labs　Deputy Director

- **Steering Committee Chair:**

  Jesse Fang

  RISC-V Foundation China Committee Chair

  Senior Vice President of Intel, Managing Director of Intel Labs China

  Tangram Technologies CEO/Chairman of Board
- **Program Committee Chair:**

  Yungang Bao

  China RISC-V Alliance Secretary-General

  Institute of Computing Technology, CAS Professor

  Open Source Chip Academician Studio, Pengcheng Lab Executive Manager
- **Local Chair:**

  Victor Chan

  Tsinghua-Berkeley Shen Zhen Institute Vice President

Prgram Committee

- Charlie Su Andes Technology
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- Weimin Dai VeriSilicon
- Donglai Dai Tangram Technologies
- Zhenbo Hu Nuclei System Technology
- Jianyi Meng Pingtou Ge(Brother Pingtou) Semiconductor
- Wei Song Institute of Information Engineering, CAS
- Dan Tang Institute of Computing Technology, CAS
- Yanjun Wu Institute of Software, CAS
- Cissy Yuan RiVAI Technologies

We invited the following **Keynote Speakers**:

- Dave Patterson, Berkeley Professor & 2017 Turing Award
- Calista Edmond, CEO of RISC-V Foundation
- Ted Speers, VP of Micro-Chip & RISC-V Board member
- Shijiang Wang, Director of Saidi Research Institute
- Alex Wang, Chairman of RISC-V Taiwan Alliance

Topics

The Forum will include a full range of plenary keynotes, academic sessions, and social events. Oral presentation and posters on high-level overview, forward thinking, groundbreaking ideas, and specific technical challenge are all positively encouraged. The speaking lineup and program are selected based on the topic/content submitted and the speaker's qualifications by the program committee. The topics include but not limit to:

- RISC-V core design, including Out-Of-Order, Low-power, ….
- RISC-V System SW, including compiler, debugger, OS, profiler, ...
- Design tools, Open Source EDA, such as RTL simulator, DFT,…
- Domain Specific Architecture like AI, IoT, Self-Drive Car, ….
- Based on RISC-V core SoC design
- RISC-V application lib standard interface
- Education on RISC-V

Submission Guideline

- Papers must be submitted in PDF format and should contain **a maximum of 2 pages** of single-spaced two-column text, excluding references.
- No specific template, but ACM template is recommended.
- Both unpublished and published papers/technical reports.
- Reviewing will be OPR (Open Peer Review). **The author list and contact information (email address) should be included** in the paper.

Submission: Oct 20,2019 AOE

Notification: Oct 27,2019 AOE

Submission Link：https://easychair.org/conferences?conf=crvf2019

Any questions on CFP and submission, please contact: xiebiwei(at)ict.ac.cn .

Besides, we also have **Panel Discussion** on RISC-V ecosystem in China:

- Chip design industry and Fab
- HW and SW ecosystem
- Impact to IT industry and communication industry in China
- Information security