SecLabel: Enhancing RISC-V Platform Security with Labelled Architecture

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Outline

- Introduction
- Pointer Integrity
- Memory Boundary Protection
- Dynamic Taint Analysis
- Implementation
- Conclusion

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Introduction

- The RISC-V architecture is well-known for its open nature.
  - Open Source, No License fee
  - Open to new design and extension

- Open to challenge.
  - Security problems in x86 and ARM architecture remains on RISC-V platforms.
  - E.g., pointer integrity, memory boundary protection, and dynamic taint analysis.

Introduction

Any effective defense on RISC-V?

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- ***Pointer Integrity***
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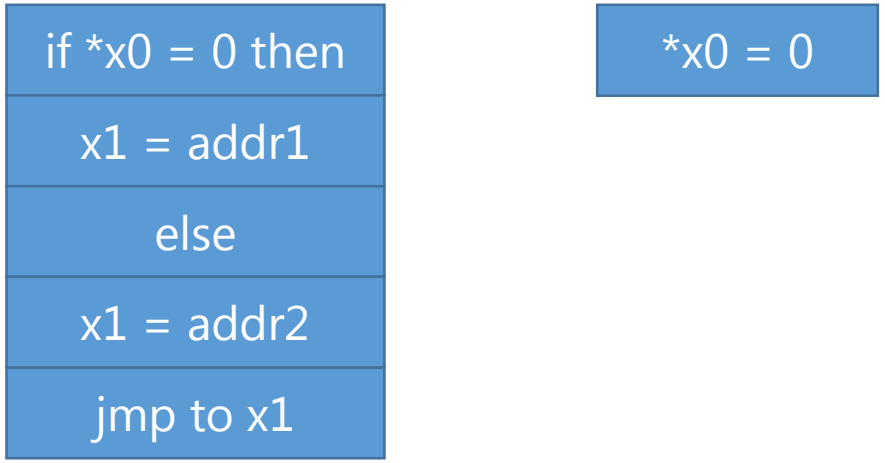
Pointer Integrity

- To ensure that the pointer is not corrupted.
  - Code-pointer Integrity and Data-pointer Integrity.



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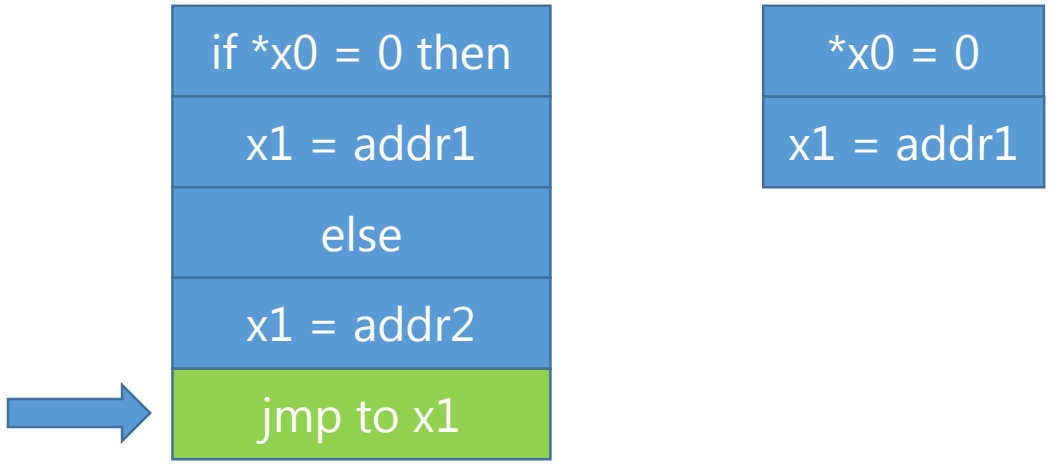

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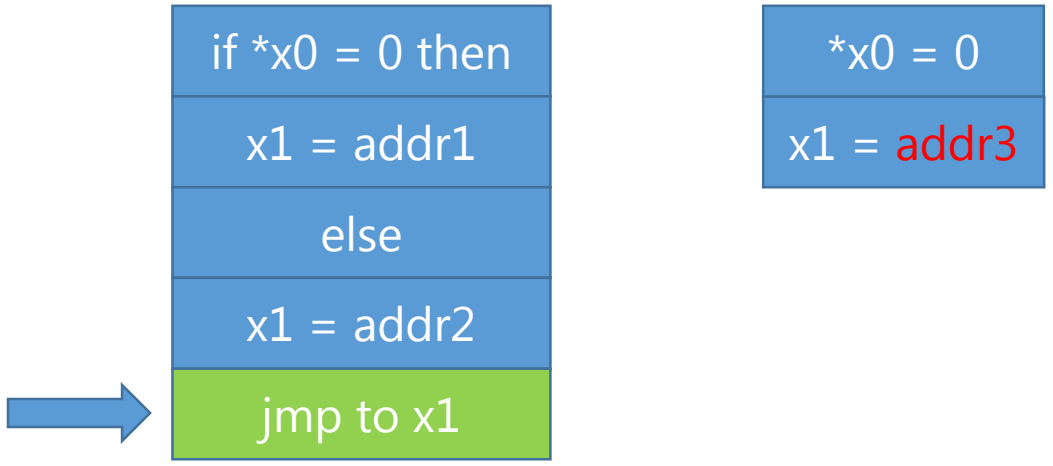

Code-pointer Attack

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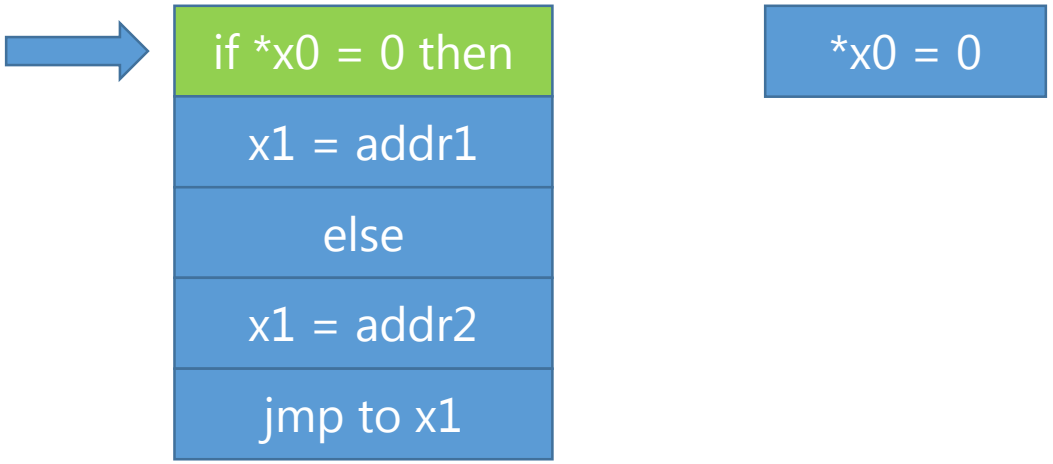

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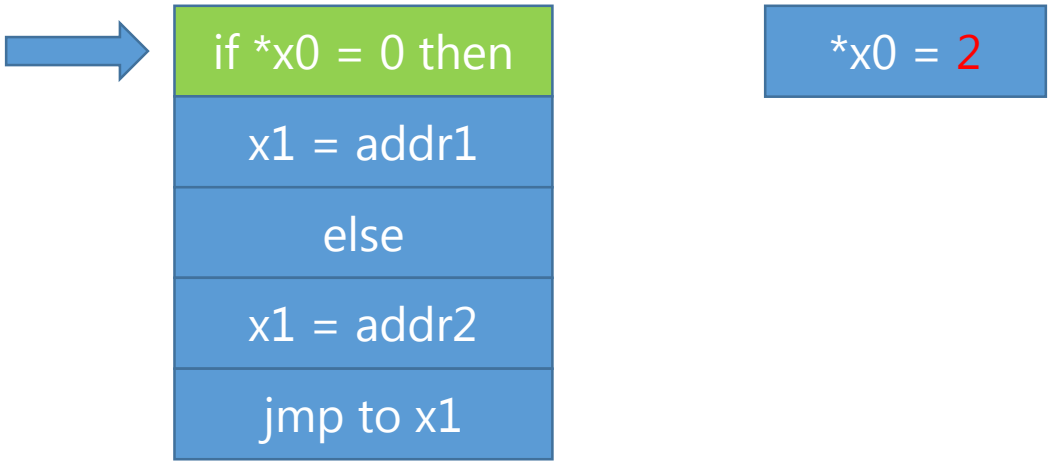

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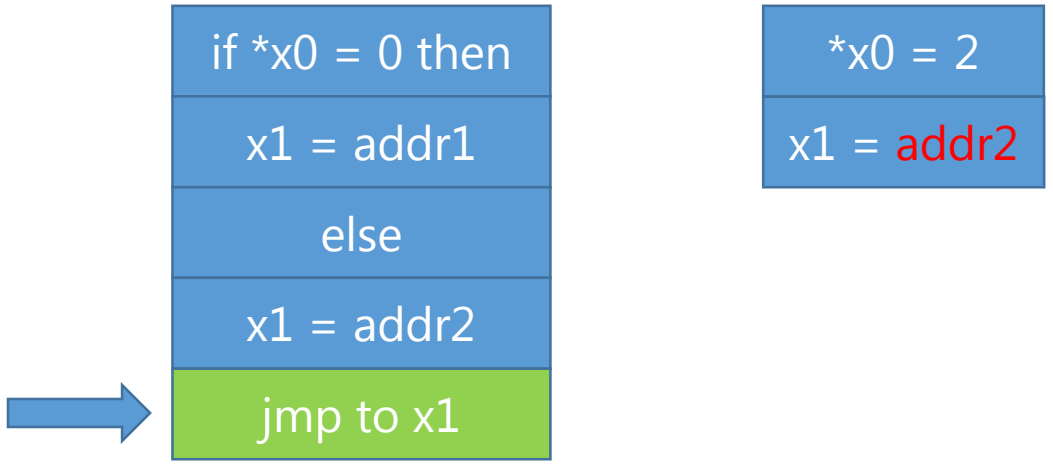
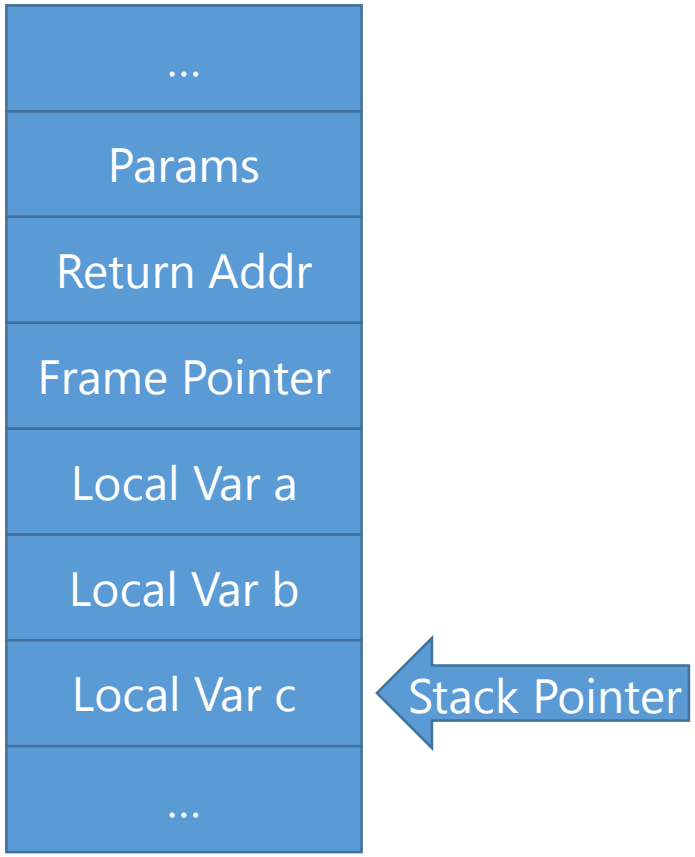


Data-pointer Attack

Pointer Integrity: Buffer Overflow

- Start of the attack: In most cases, a buffer overflow vulnerability.



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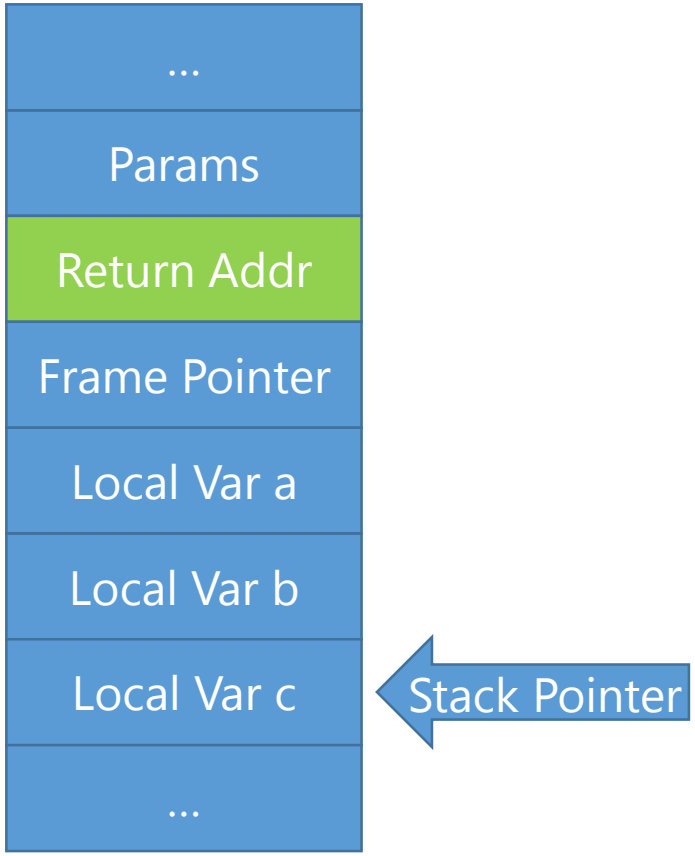

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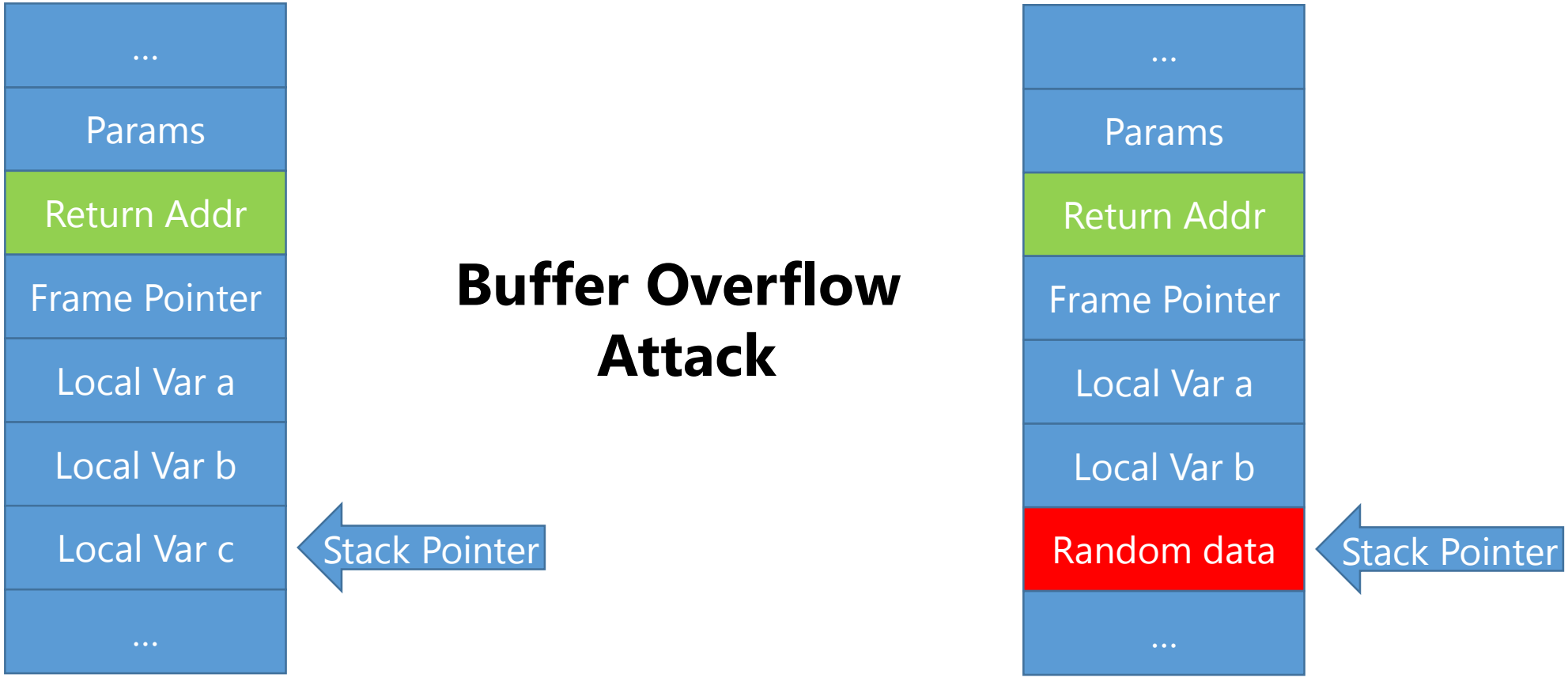

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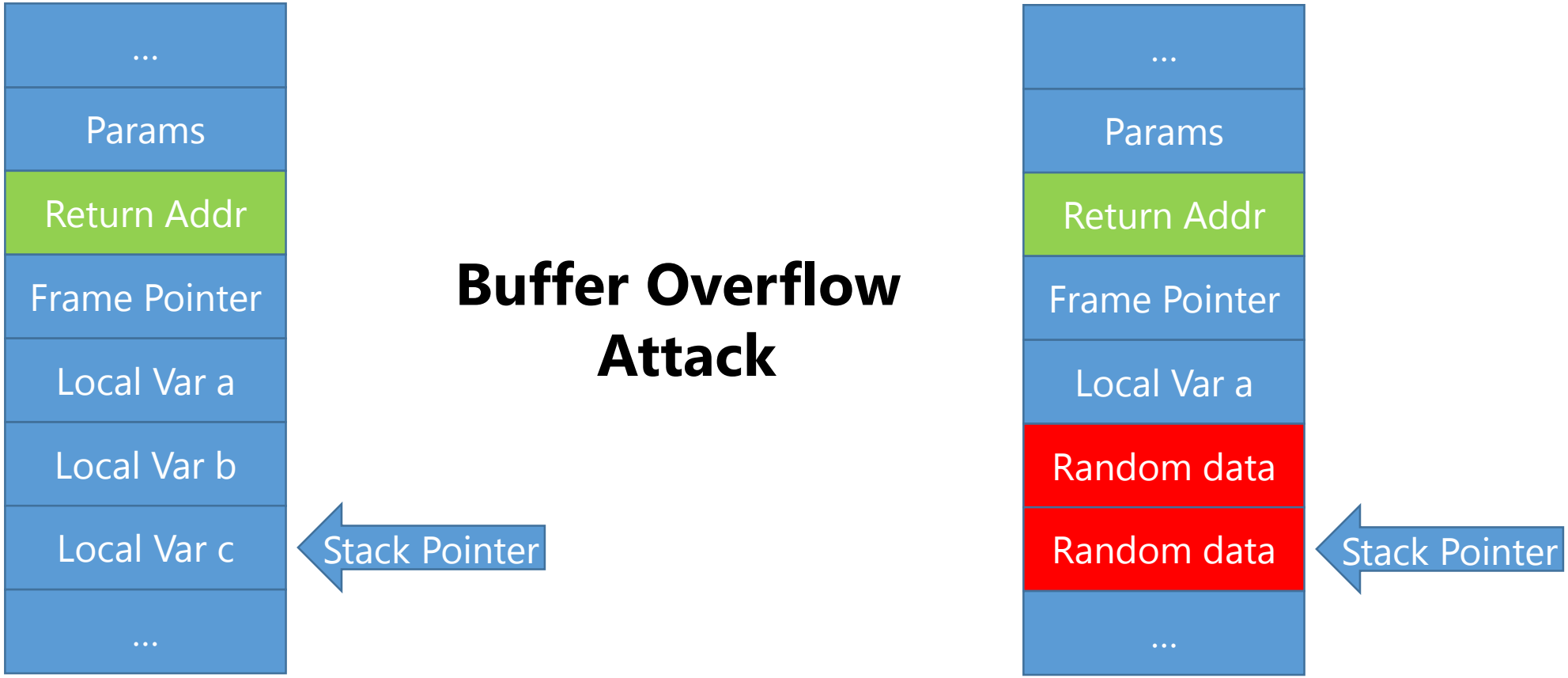

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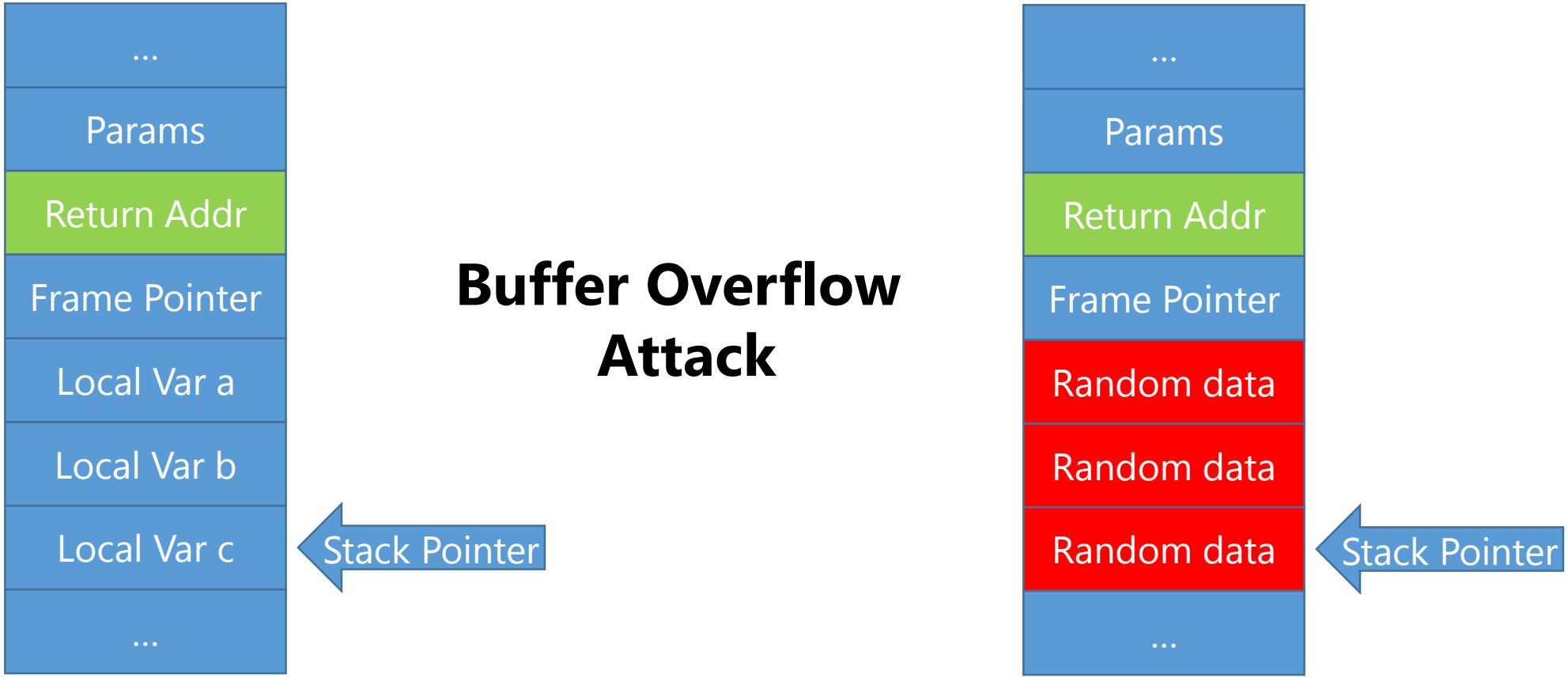

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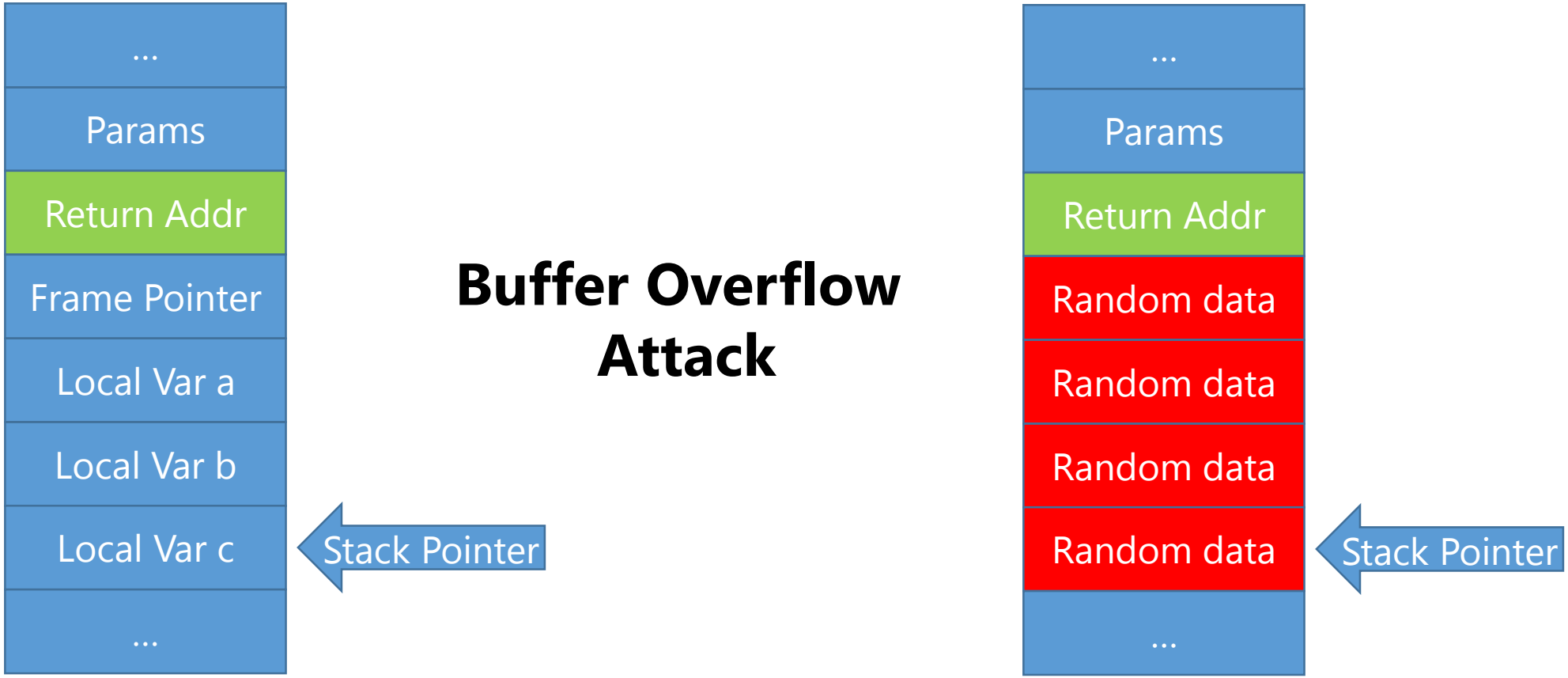

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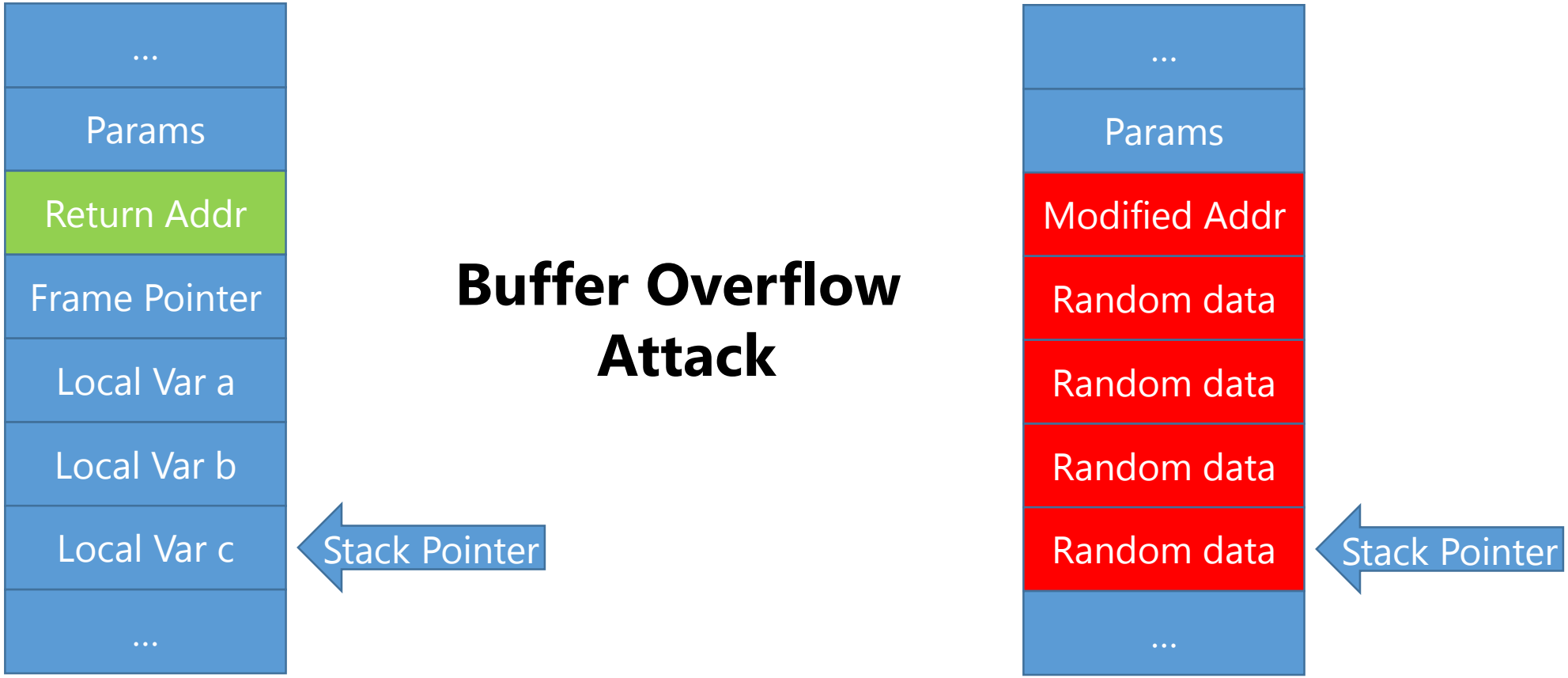
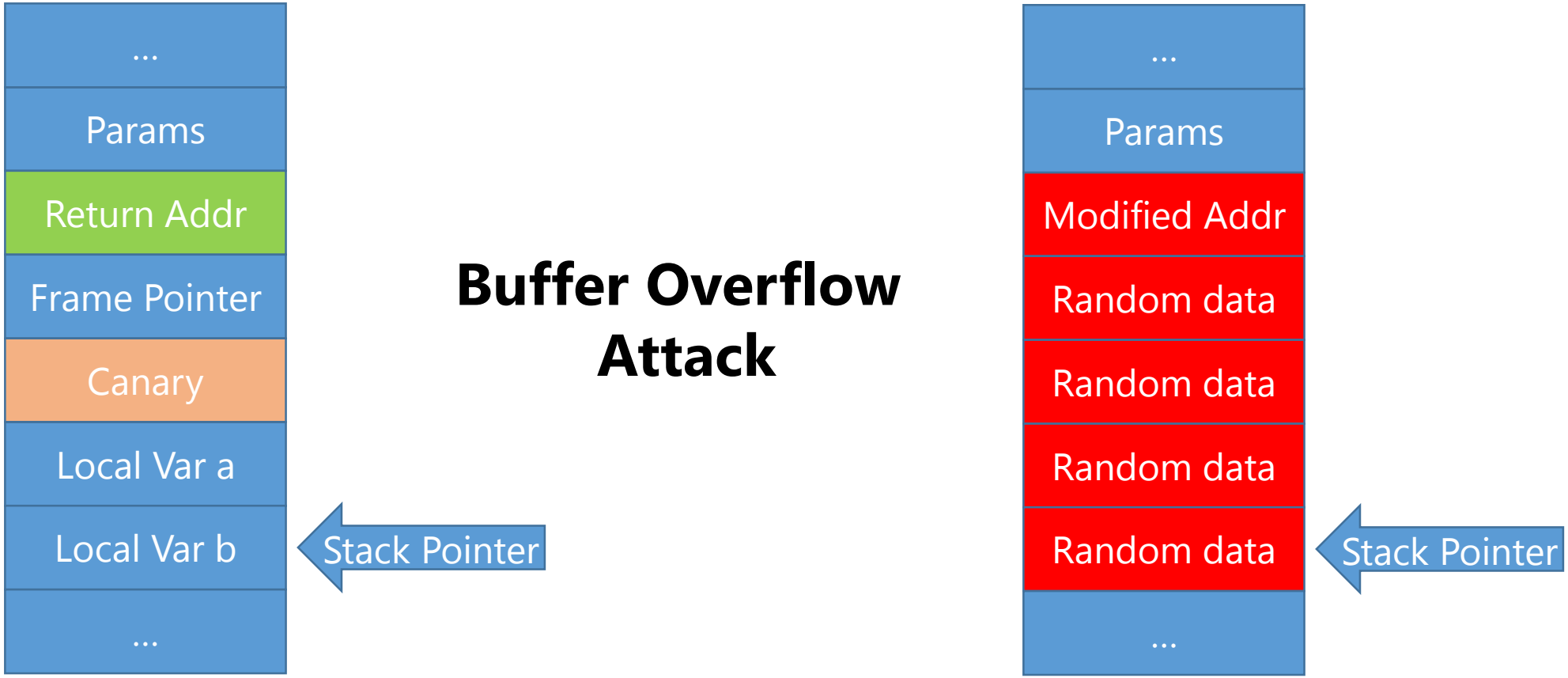


Pointer Integrity: Canary

- **Stack Canary**[1]: The most widely used defense to buffer overflow attack.



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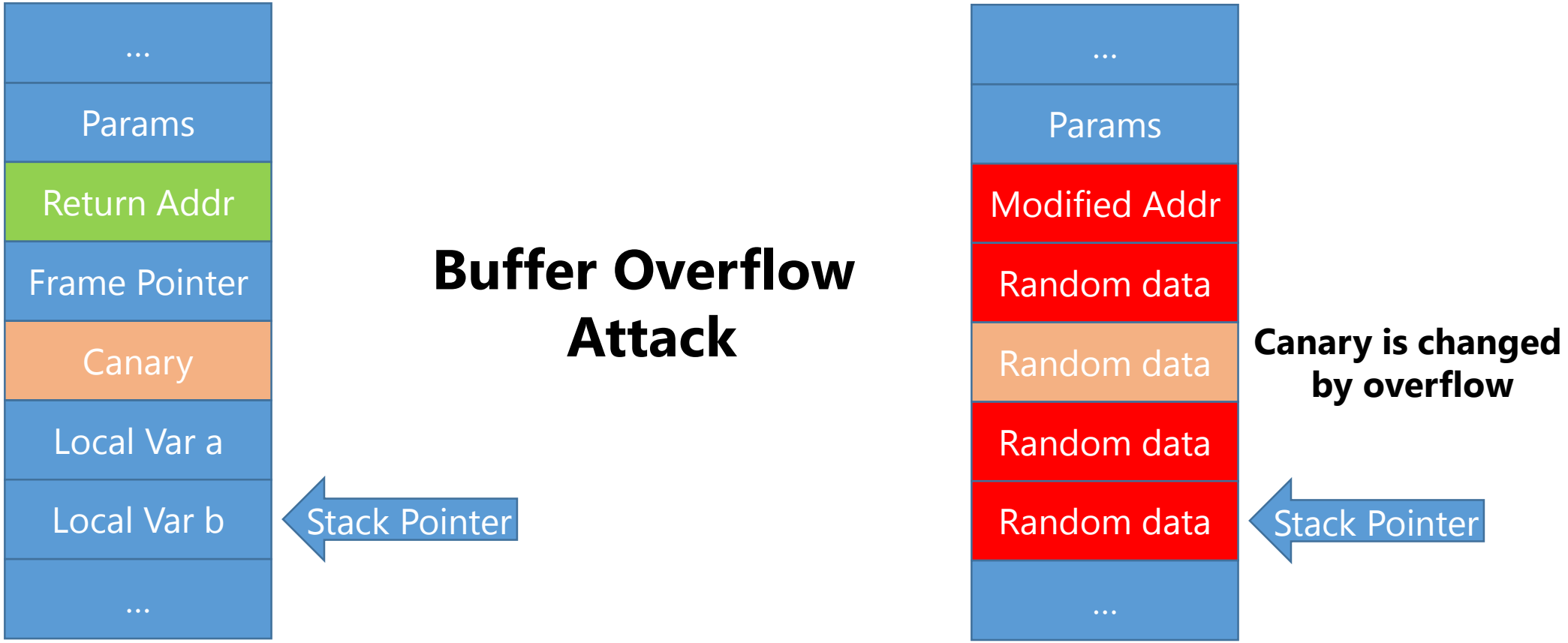


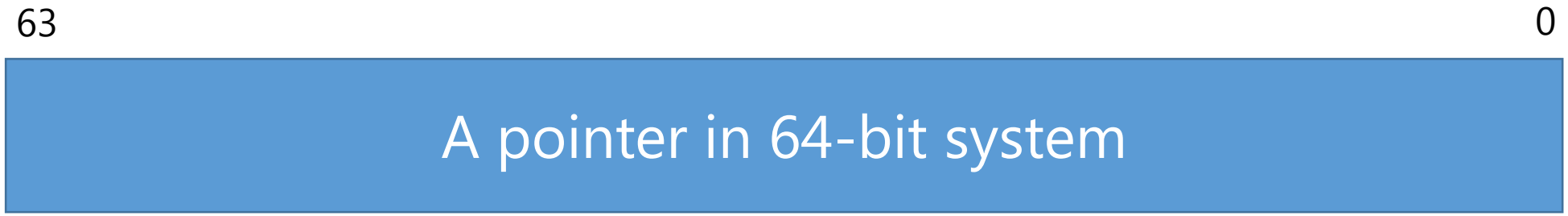
Pointer Integrity: Canary

- **Stack Canary**[1]: The most widely used defense to buffer overflow attack.

- Weakness:
  - Easy to bypass[2]
  - Not efficient to defend against data-pointer attack

Pointer Integrity: PAC

- **Pointer Authentication Code**[3] is introduced in 64-bit ARMv8.3 architecture.



Is it really necessary to use a 64-bit address?

Pointer Integrity: PAC

Is it really necessary to use a 64-bit address?

- 2^{64} bit = 16384 PB = 16.8 millions TB = 17.2 billions GB
- **Summit**: 10 PB memory
- **Sunway TaihuLight**: 1.32 PB memory
- **Linux**: Up to 128 TB virtual memory
- **Windows**: Up to 16 TB virtual memory

Pointer Integrity: PAC

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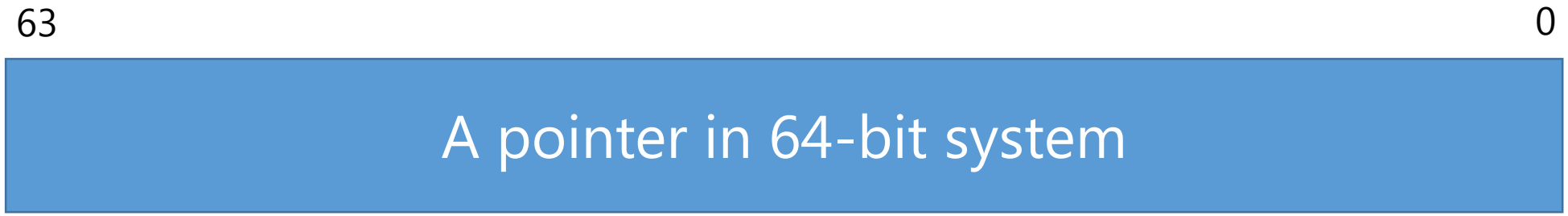

Pointer Integrity: PAC

- **Pointer Authentication Code**[3] is introduced in 64-bit ARMv8.3 architecture.

- Pointer Value + 64-bit Context Value + 128-bit Secret Key => PAC
- Up to 48 bits for virtual address, and at least 7 bits for PAC

Pointer Integrity: PAC

- PAC is good, but the deployment is painful.
  - The mechanism is released with ARMv8.3 architecture since 2016.
  - ARM does not release any processor with ARMv8.3 till now.

- The only processors with PAC support are Apple A12 and A13.
  - Closed ecosystem.
  - No available to system developers.

Pointer Integrity: RISC-V

- RISC-V based PAC
  - A group of new hardware instructions
    - Forge PAC, examine PAC, strip PAC
  - New registers for storing the 128-bit secret key
    - Secret keys for data pointers and code pointers
  - Hardware-based crypto engine
    - Generate PAC from pointer and 64-bit context value

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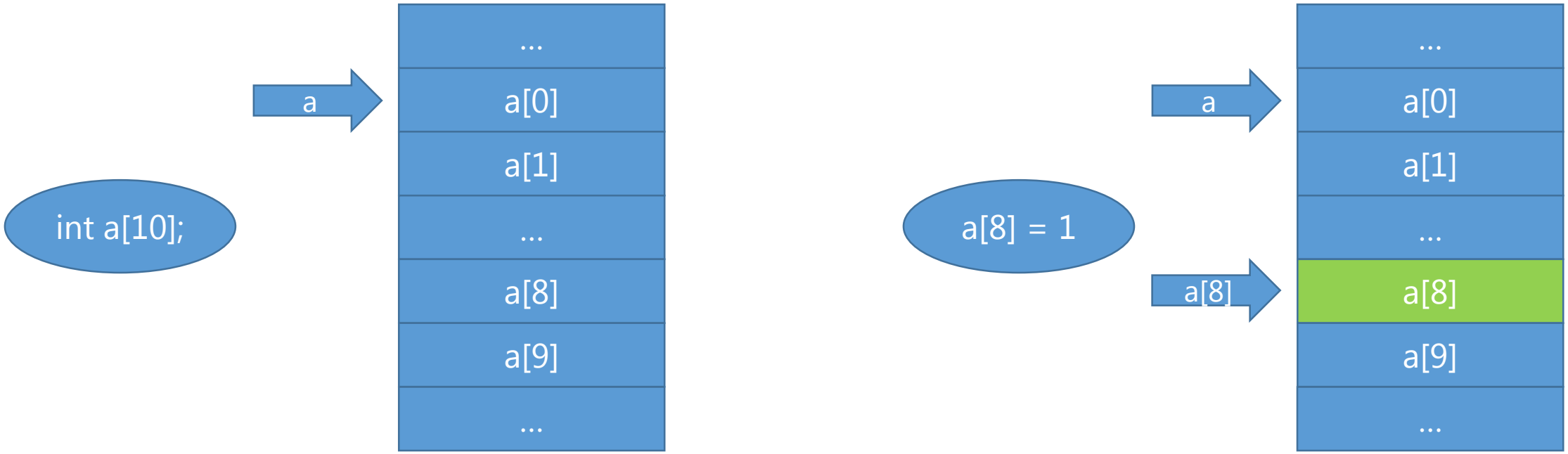
Memory Boundary Protection

- To ensure the memory access won't go out of its expected boundary.



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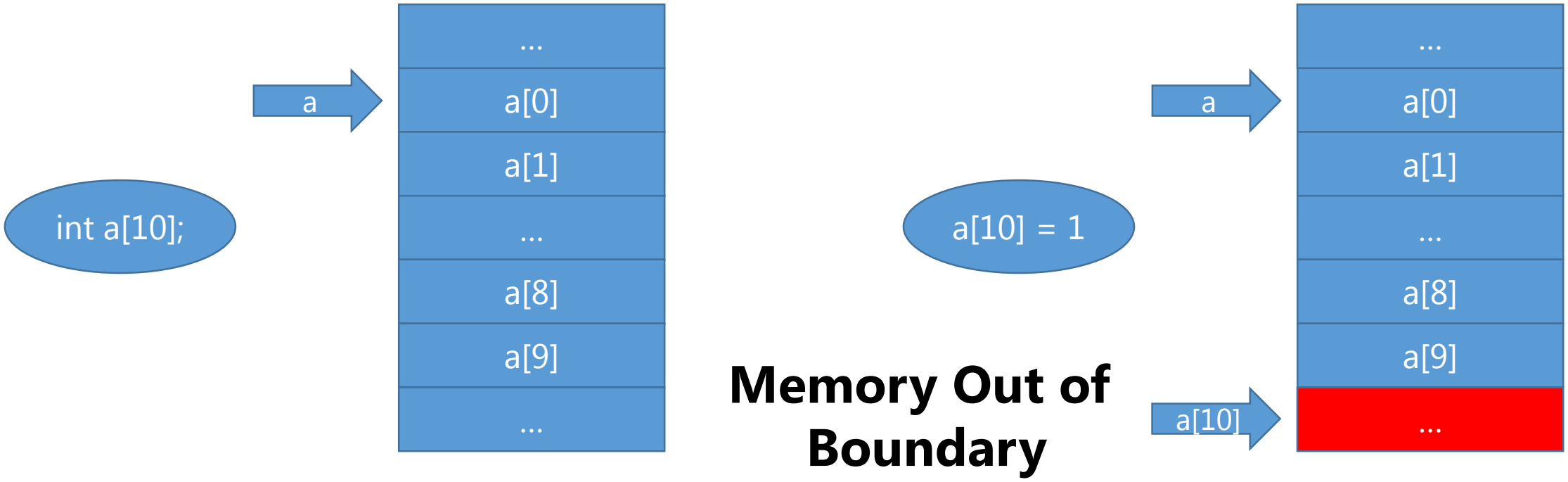
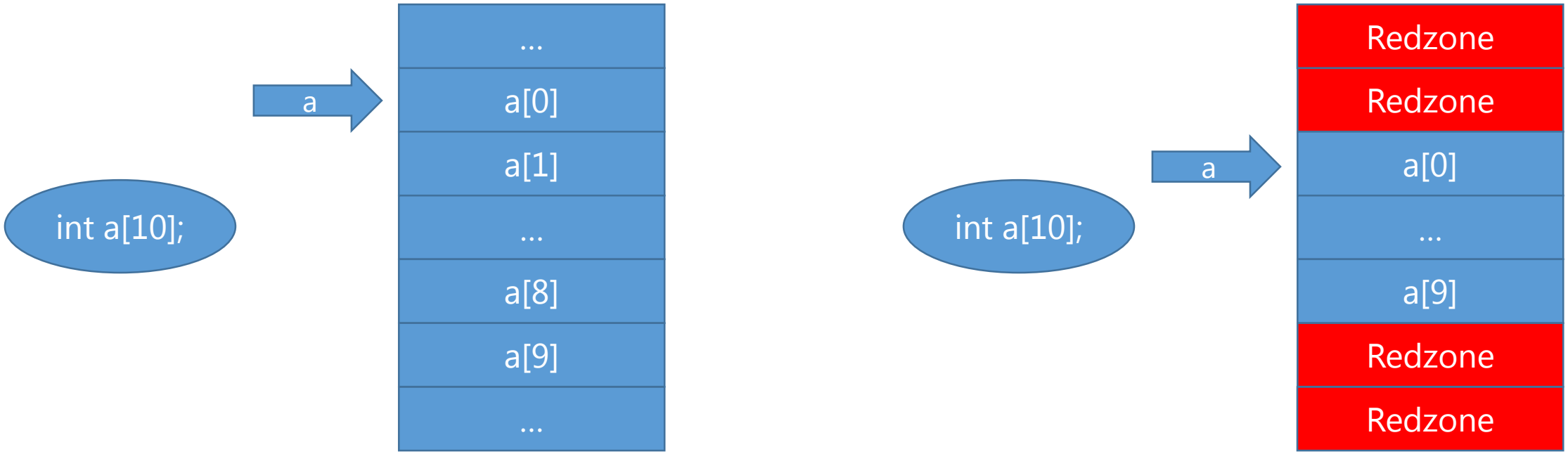


Memory Boundary Protection: Address Sanitizer

- **Address Sanitizer**[4]: Use redzones to detect out-of-bound access.



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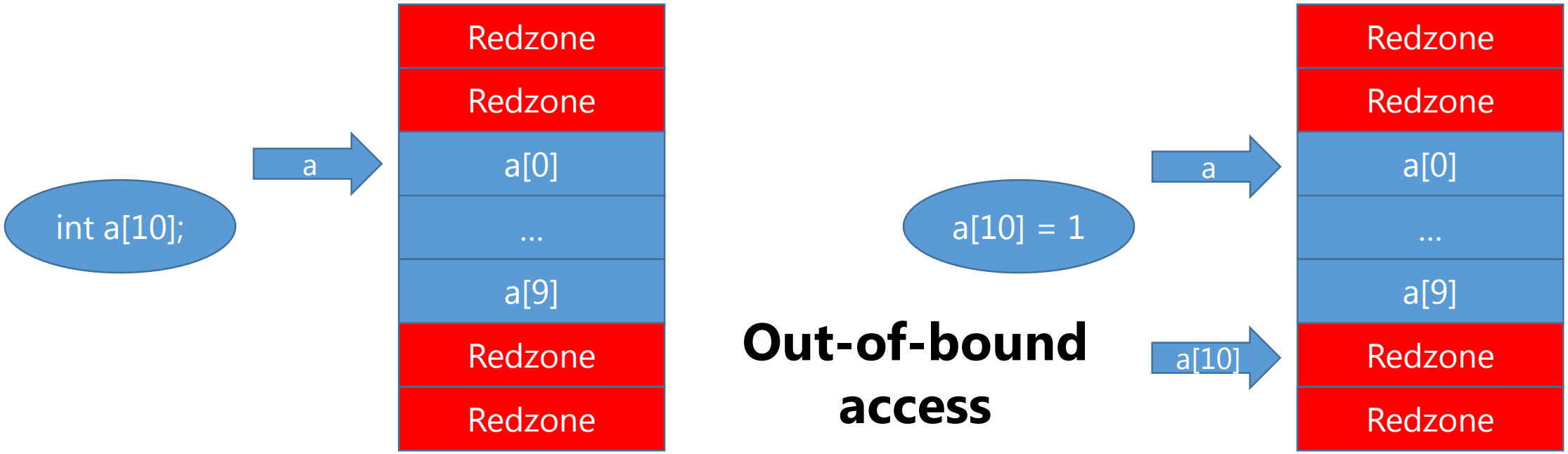


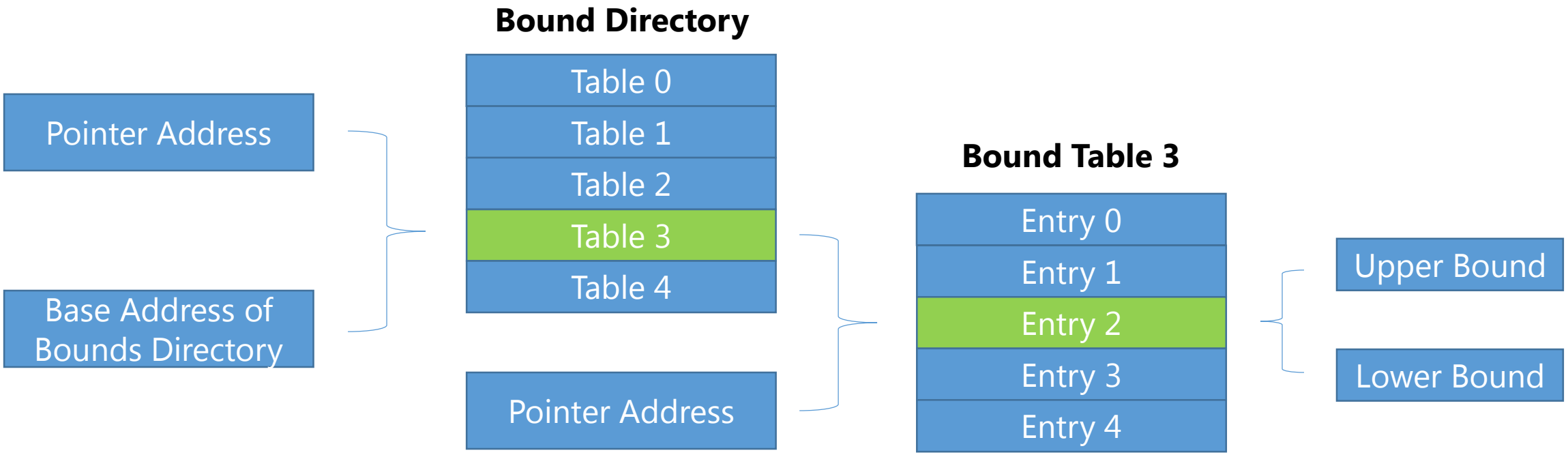
Memory Boundary Protection: Address Sanitizer

- **Address Sanitizer**[4]: Use redzones to detect out-of-bound access.

- Weakness:
  - Large memory overhead
  - Large performance overhead
  - False negative is possible

Memory Boundary Protection: Intel MPX

- **Intel MPX**[5]: An architecture extension dedicated for memory bound protection.



Memory Boundary Protection: Intel MPX

- **Intel MPX**[5]: An architecture extension dedicated for memory bound protection.

- Weakness:
  - Performance overhead for two-layer translation
  - Multithread not support
  - Not production ready, support will be removed from GCC 9

Memory Boundary Protection : RISC-V

- RISC-V based Memory Boundary Protection

- Use the head bits for memory bounds
  - 9 bits if PAC is implemented
  - 16 bits if PAC is not implemented
  - More bits in 128-bit RISC-V architecture[6]

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Dynamic Taint Analysis

- Analysis the information flow of specific objects.
  - Example scenario: Privacy leakage detection

```
……
char* password = getInput();
char* copied = copy(password);
printf(“copied: %s\n”, copied);
……
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Taint Source

getInput

Taint Sink

printf

Dynamic Taint Analysis

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Taint Path Founded!

Dynamic Taint Analysis

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Taint Source

getInput

Taint Sink

printf

Tainted Variable

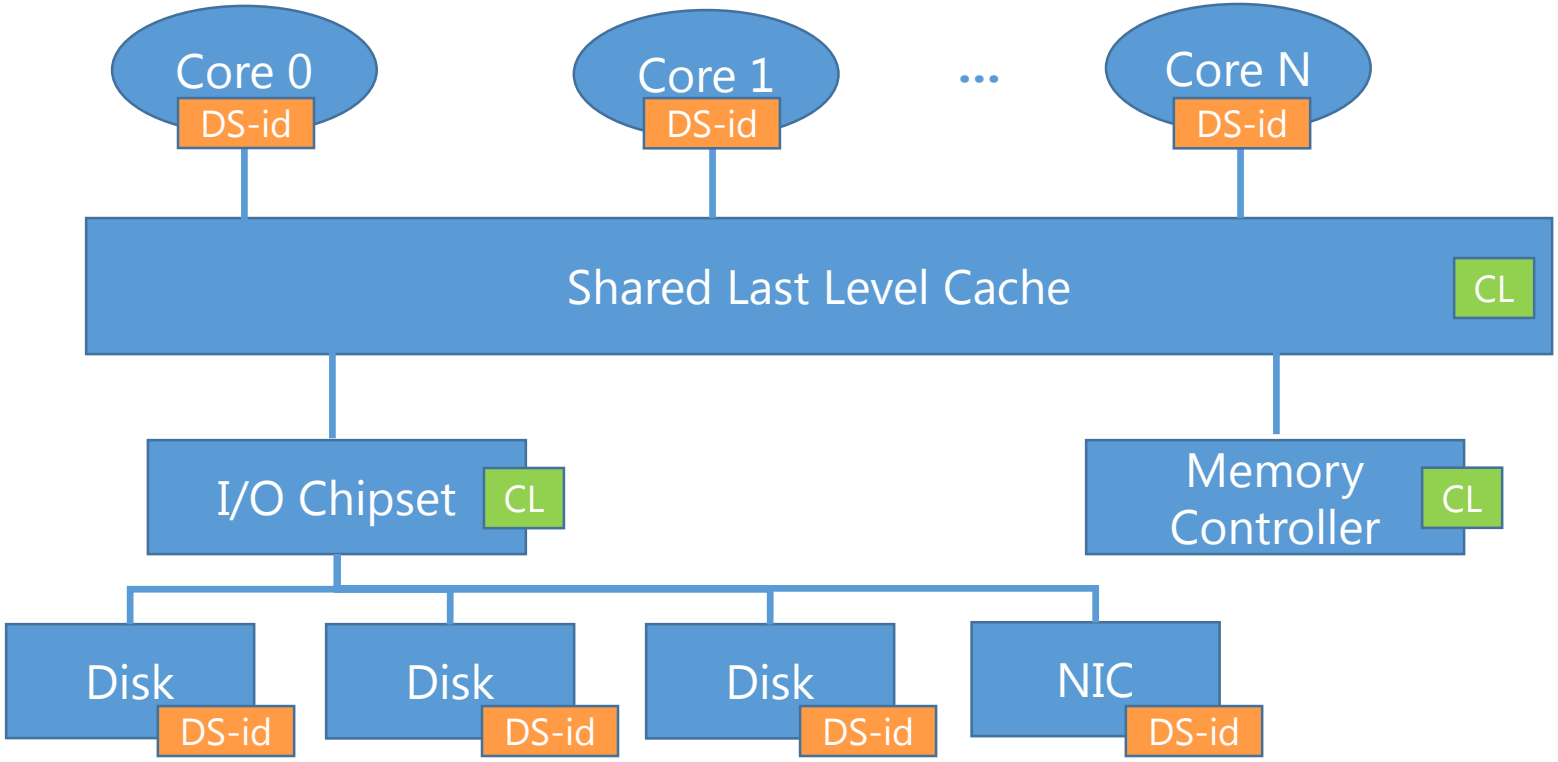
password

copied

- How to learn the taint propagation from *"password"* to *"copied"*?
  - Heavy instrumentation
  - Add tons of instructions to monitor the data flow

Dynamic Taint Analysis

- **Labelled RISC-V Architecture**[7]: Every hardware request is attached with a label.



Dynamic Taint Analysis

- **Labelled RISC-V Architecture**[7]: Every hardware request is attached with a label.
- Use the label to represent taint flag
  - Automatically propagation via hardware support
  - No instrumentation required
- Use the Control Logic (CL) to achieve detection

What about the propagation outside of hardware request?

Dynamic Taint Analysis

What about the propagation outside of hardware request?

- Allocate a few bits from the unused bits in 64-bit pointer
  - In coarse-gained analysis, 1 bit is sufficient
  - This bit automatically transfers during the execution of data operation instructions.
  - Feed to the *DS-id* register during hardware request

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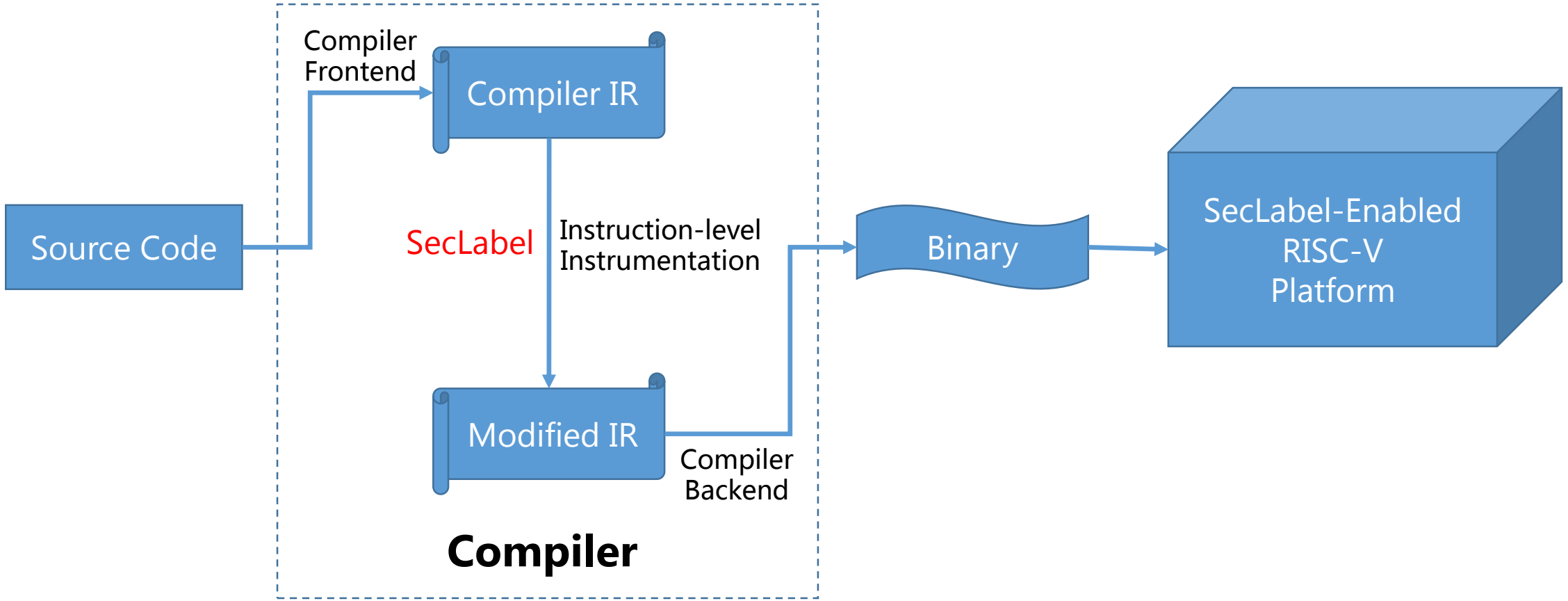
Implementation

- **SecLabel:** Enchancing RISC-V Platform Security



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Conclusion

- In light of the PAC in ARMv8.3, we can leverage the open feature of RISC-V and implement similar mechanism for pointer integrity.

- With addition bits in the head of a pointer address in 64-bit or 128-bit RISC-V architecture, an enhanced memory boundary protection can be deployed.

- Combining the labelled RISC-V architecture and unused bits in an address, we are able to facilitate the existing dynamic taint analysis.

Reference

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Thanks!

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