Rebuild IC Front End with Chisel: An Example Study of RISC-V Vector Processor

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Outline

1. Lightening Slide
2. Computation Paradigm Change
3. Design Methodology Change
4. A RISC-V Vector Processors Generator
5. How We Collaborate on RISC-V Vector

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Lightening Slide

Three Changes in IC Industry

Rebuild IC Front End with Chisel: An Example Study of RISC-V Vector Processor

Computation Paradigm

- Symbolism ⇒ Connectionism

Design Methodology

- Verilog ⇒ Chisel

CPU Architecture

- Scalar ⇒ Vector

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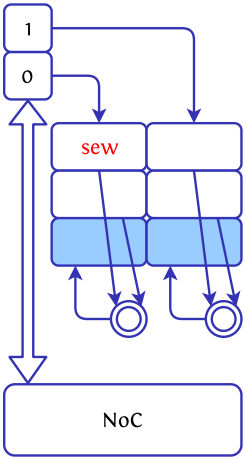
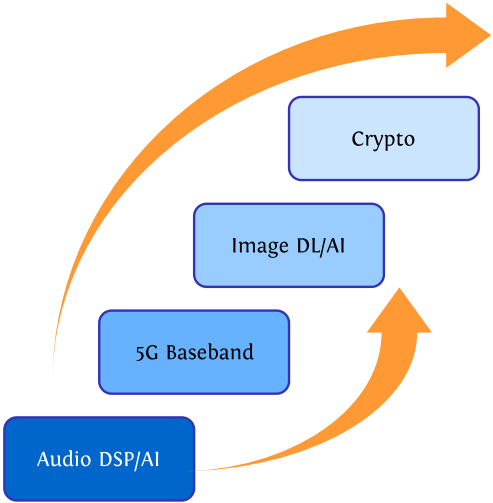
SiFive China Vector Processor Roadmap

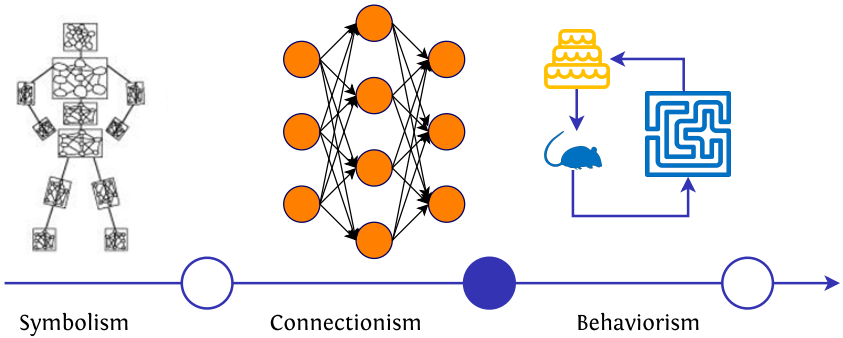




Computation Paradigm Change

Computation Paradigm Change

Logic-based computation ⇒ raw-data-based computation



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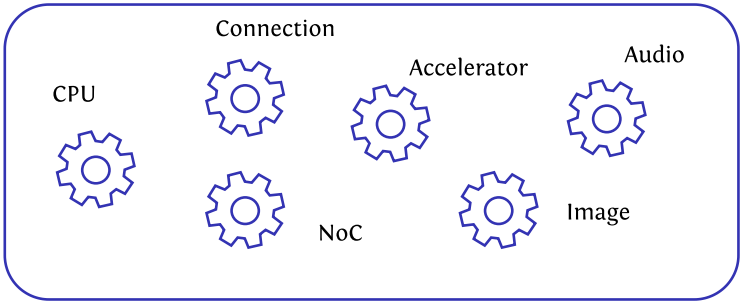
Design Methodology Change

Productivity Change

Company-wide local workspace ⇒ cross-company cloud workspace



Cloud workspace with Chisel

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Chisel and Related Tool Set

Tool	Changes	Key importance
Chisel	Space programming	Describe graph, NOT behavior
Treadle	Simulation	Easy cloud deploying
Chisel.testers	Verification	Enable complex model in Scala
Firrtl	Synthesis	Open standard and compiler framework
Diplomatic TileLink	SoC integration	Dynamic SoC and NoC generation
Wit/Wake	IC workflow	Hash-chain to standardize IC tools

Berkeley Sifive	IC industry	Copy to China

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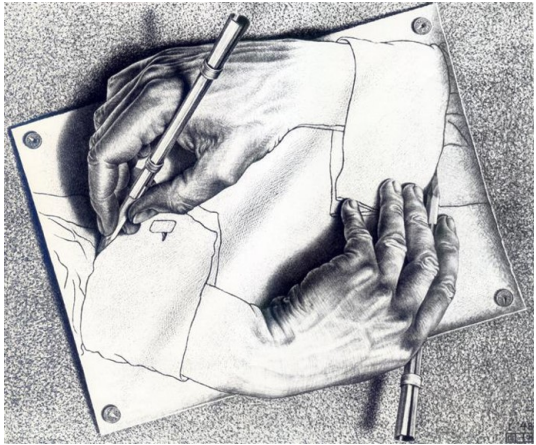
Why Copy-to-China

Rebuild IC Industry with AI

- AI explore IC design space
- Chisel is the interface for AI to access IC



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A RISC-V Vector Processors Generator

Why RISC-V Vector ISA Matters

X86	ARM	RISC-V
		
PC Scalar	Mobile Scalar	AI-IoT Vector
Symbolism	Symbolism	Connectionism

Comparision of RISC-V Vector & GPU & ASIC

GPU

- It is huge, and hungry.

ASIC

- It is slow and fragmented.

RISC-V Vector

- It is unified programmable.

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RISC-V Vector ISA Introduction

- 367 vector instructions VS 296 scalar instructions

Config	`setvl/setvli` vtype (vsew, vlmul) and vl (length)
Load/store	unit stride, stride, indexed and first fault
Atomic OPs	atomic memory read-modify-write
Integer	logic, bitwise, and integer arithmetic
Fixed-point	fixed-point arithmetic
Floating-point	floating-point arithmetic
Reduction	reduce a vector to a scalar
Mask	mask helper instructions
Permutation	move element around in a vector

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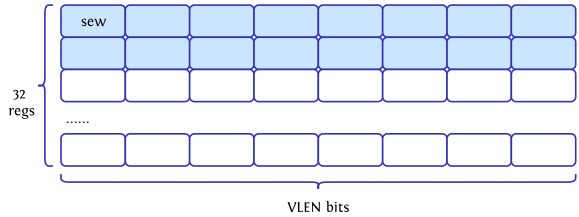
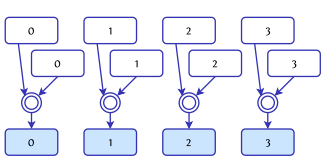
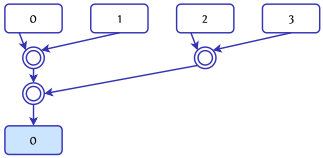
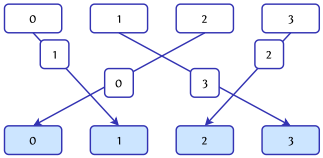
RISC-V Vector Register File and Computation









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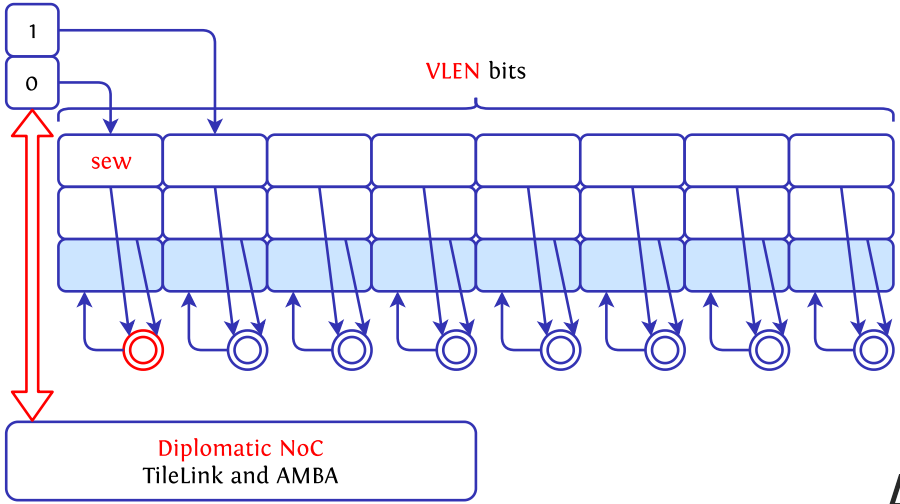
A RISC-V Vector Processors Generator



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Sand: Chisel-based RISC-V Vector Formal SPEC

- Inspired by RISC-V Scalar SPEC $^{\alpha}$

Forvis	BlueSpec	Haskell
Grift	Galois	Haskell
Sail	Cambridge	Sail
Riscv-plv	MIT	Haskell
Kami	SiFive	Coq

- Why not a SPEC in the design language?

Sand	SiFan	Chisel

- Easy to read, check and reference
- Synthesizable verification

α https://github.com/riscv/ISA_Formal_Spec_Public_Review

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How We Collaborate on RISC-V Vector

How We Collaborate on RISC-V Vector

Program in RISC-V V

- Try Spike
- Try GCC assembler

Execute on Rock

- Sand, introduced
- Rock, on the way

Explore new market

- AI
- 5G
- Crypto

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