

EXPANDING RISC-V ECOSYSTEM WITH VEGABOARD / VEGA-LITE

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Nov 2019



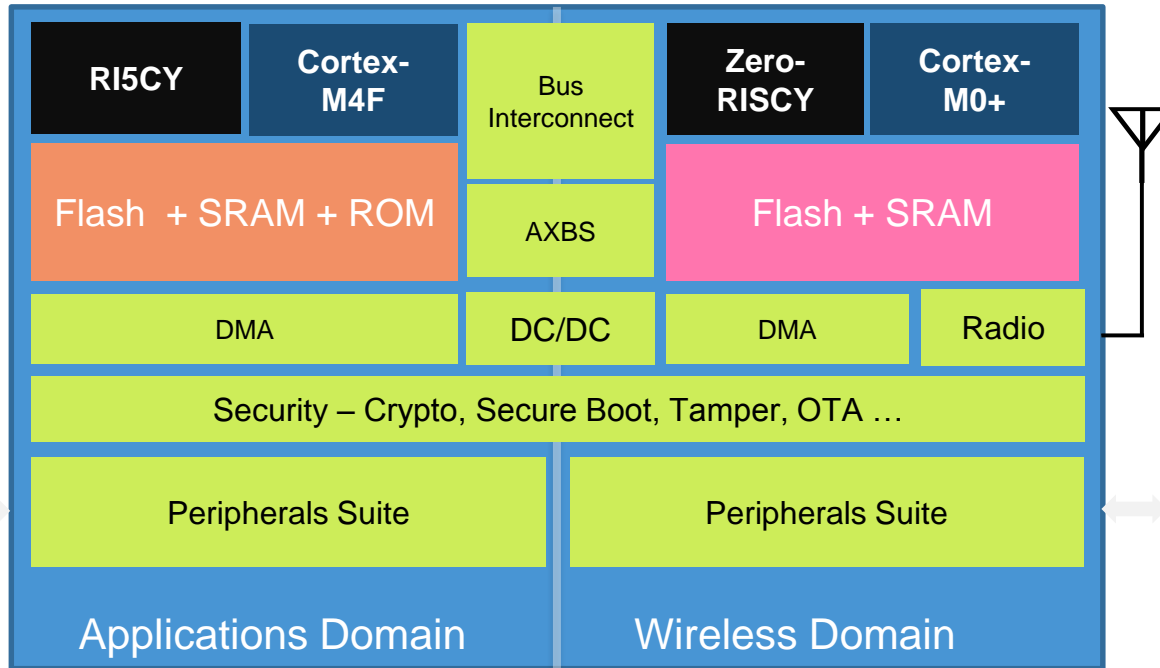
SECURE CONNECTIONS
FOR A SMARTER WORLD

Ecosystem Is Very Important to RISC-V



- Wide ecosystem is one of the key factors of ARM's success
- We believe ecosystem is key to the success of RISC-V
- As a Platinum Member, how can NXP facilitate a deep ecosystem for RISC-V? Practice to know the truth.

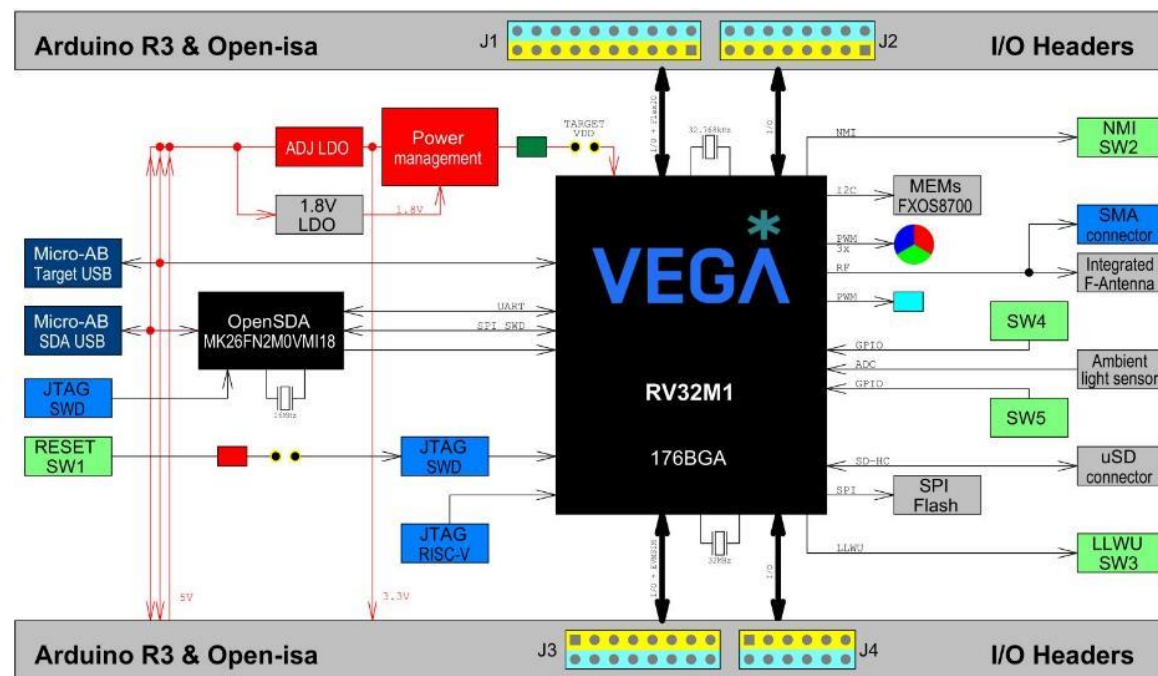
RV32M1 SOC



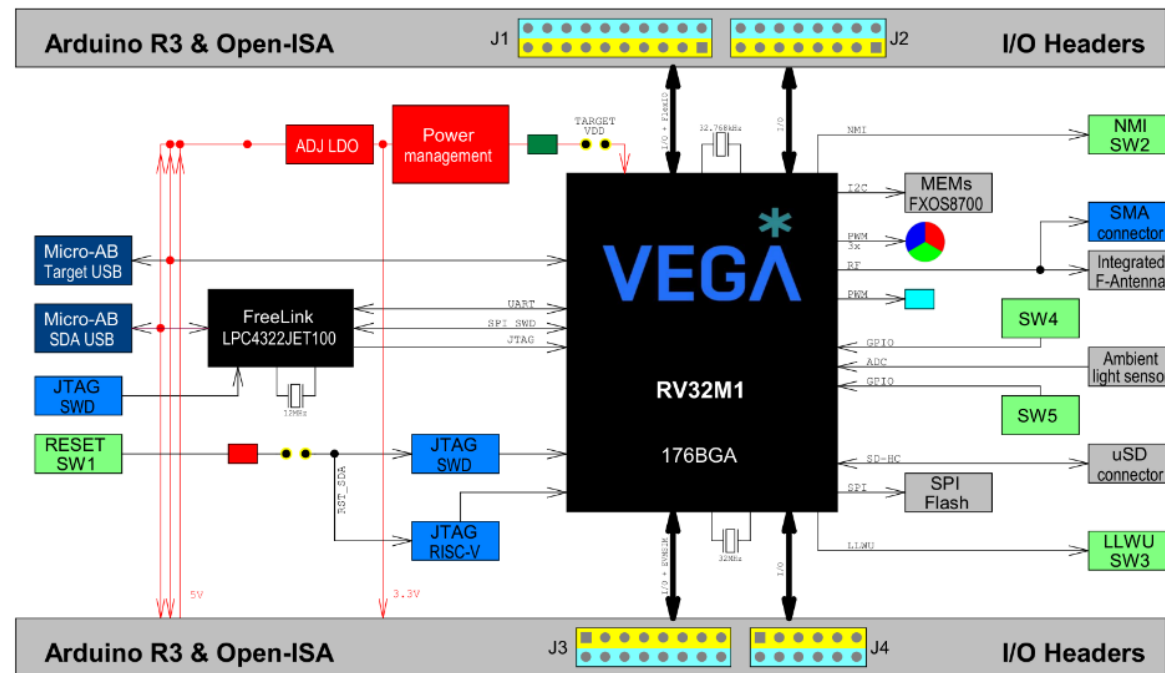
- Intended only as silicon evaluation vehicle
- Not for SALE!

- 4 CPU cores, up to 72MHz
 - One RISC-V RI5CY and one RISC-V ZERO_RISCY
 - One ARM Cortex-M4F and one Cortex-M0+
 - Easiest way to compare ARM vs RISC-V side by side
- Low power consumption and high integration
 - Support BLE、Generic FSK, 802.15.4
 - Security engine include AES128/196/256, DES/3DES, SHA-256, RSA and ECC PK-256/Curve25519
 - USB2.0 FS、SAI support I2S and AC'97、SDHC、EMVSIM
 - 1x32ch FlexIO、4xUART、4xI2C、4x16-bit LPSPI、1x12bit ADC
 - 2x6ch的PWM , 1x2ch的PWM , RTC , LPTimer
 - 1.25 MB Flash 、 384 KB SRAM

VEGAboard / VEGA-Lite -- Full-Featured RISC-V Dev Platform

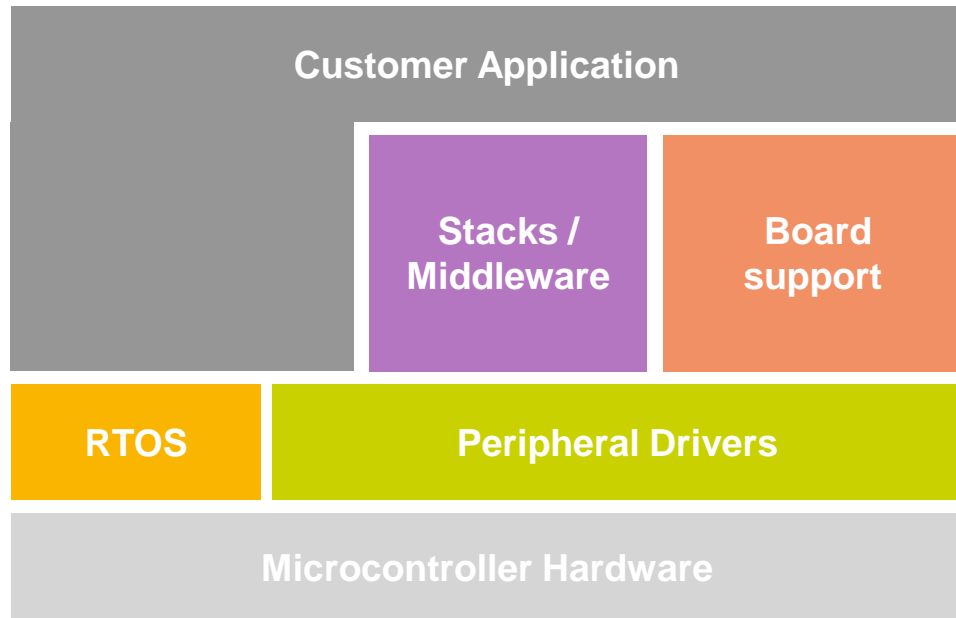


VEGAboard



VEGA-Lite / 织女星开发板

SDK for VEGAboard / VEGA-Lite



Features

Architecture:

- Single driver for each peripheral
- Transactional APIs w/ optional DMA support for communication peripherals

Integrated RTOS:

- FreeRTOS v9
- RTOS-native driver wrappers

Integrated Stacks and Middleware

- USB Host, Device and OTG
- BLE stack
- Amazon Web Service IoT
- QCA WiFi Stacks
- lwIP, FatFS
- Crypto acceleration plus wolfSSL
- SD and eMMC card support

Reference Software:

- Peripheral driver usage examples
- Application demos
- FreeRTOS usage demos

License:

- BSD 3-clause for startup, drivers, USB stack

Toolchains:

- Eclipse IDE
- GCC w/ Cmake

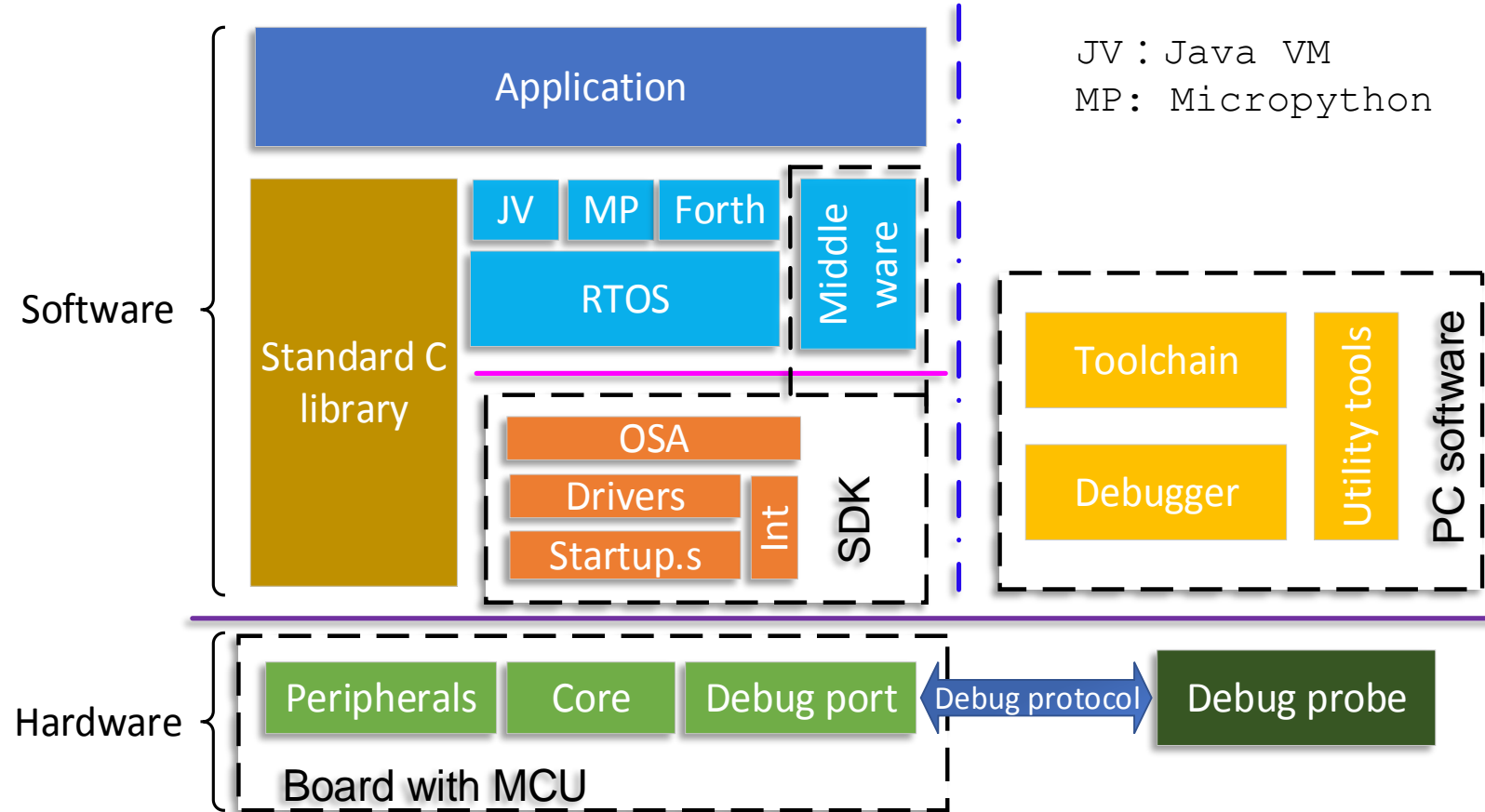
Quality

- Production-grade software
- MISRA 2004 compliance
- Checked with Coverity® static analysis tools

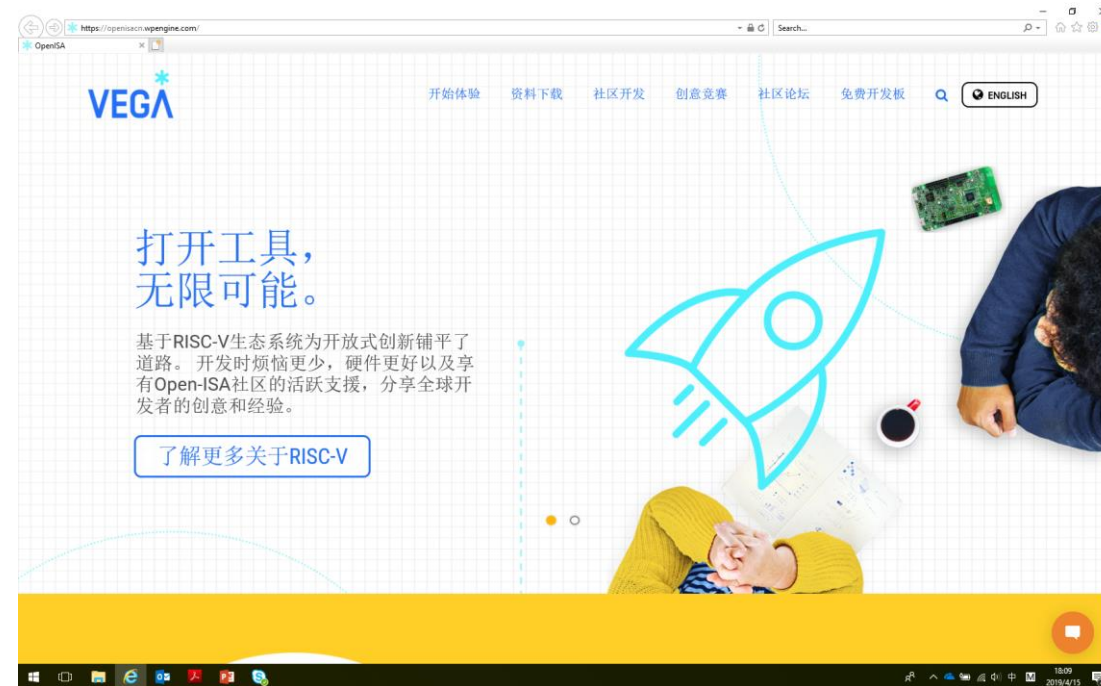
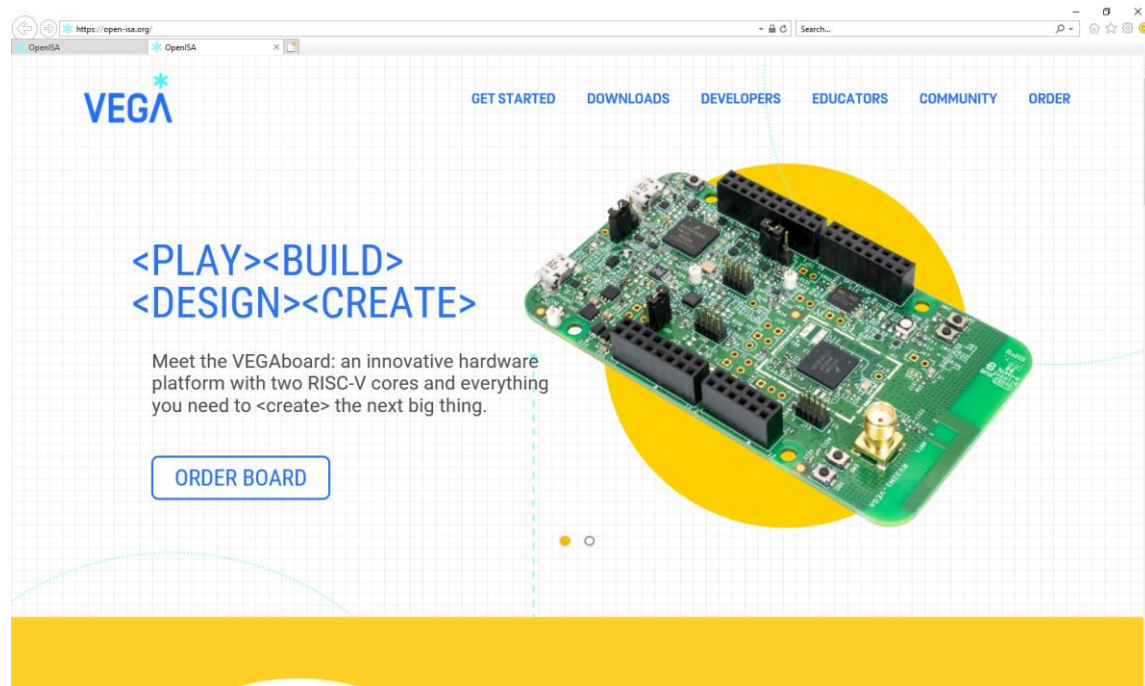
Development based on VEGAboard / VEGA-Lite



- Development Tools
 - Eclipse IDE
 - GNU GCC RISC-V toolchain
 - OpenOCD debugger
- Software
 - SDK from OPEN-ISA with drivers, middleware and examples
- Application development
 - Consistent with general MCU



www.open-isa.org / www.open-isa.cn



Interaction with Ecosystem

 **RISC-V[®]**
DEVELOPERS

Open enablement, infinite possibilities.
Pave the way for open innovation using
the RISC-V ecosystem. See what you can
do with the VEGAboard's full-featured
MCU, running an open ISA.

[LEARN MORE](#)

ETH zürich


SYSTEMS



amazon



expresslogic

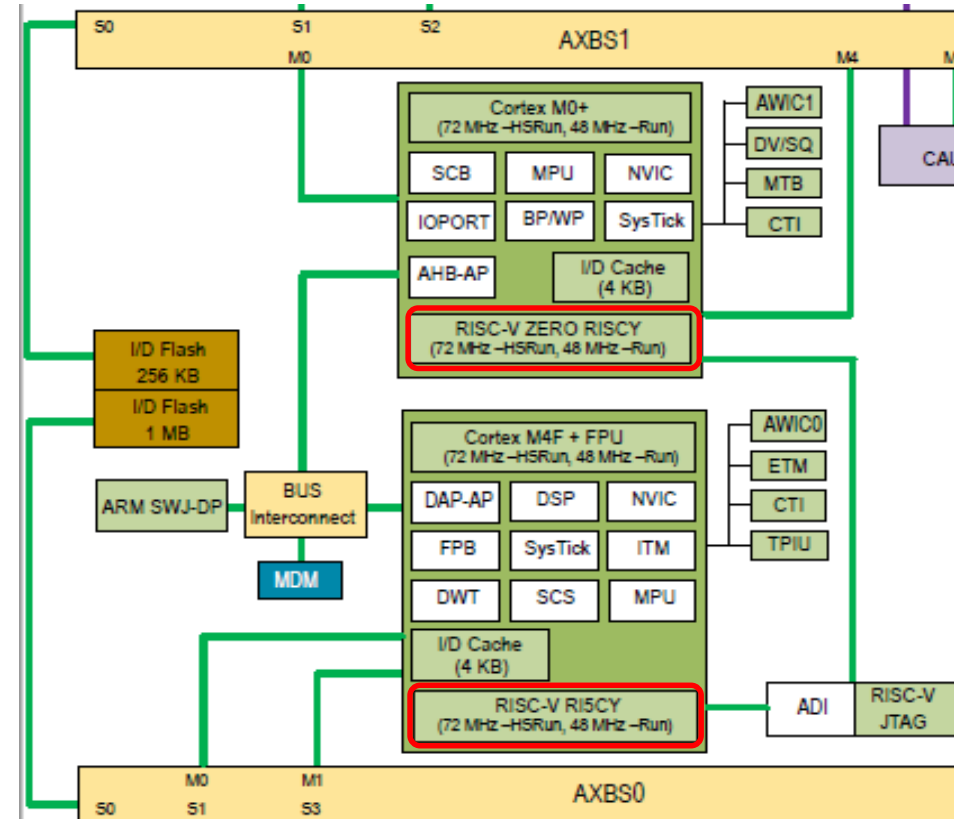
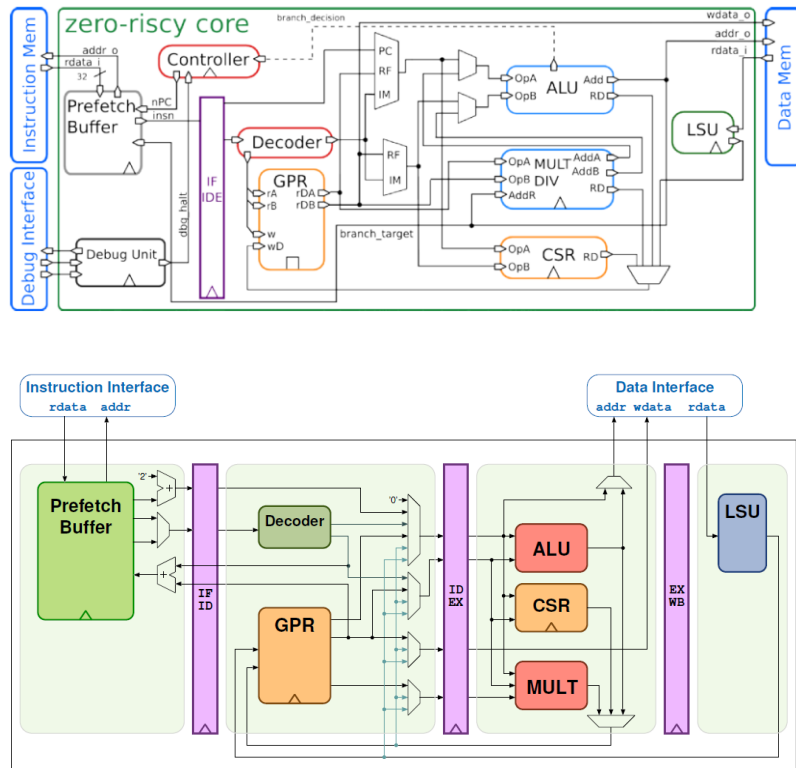


 ASHLING


Alibaba Cloud

 **RT-Thread**
小而美的物联网操作系统

PULPino Cores



- Evaluated several open source cores from the community
- Leveraged RI5CY & Zero-riscy cores in our RV32M1 SoC
- Found & fixed bugs in the core design and contributed back to the community

Toolchain Evaluation and Enhancement

- We've evaluated following toolchain on VEGAboard / VEGA-Lite

- GCC
- IAR
- LLVM

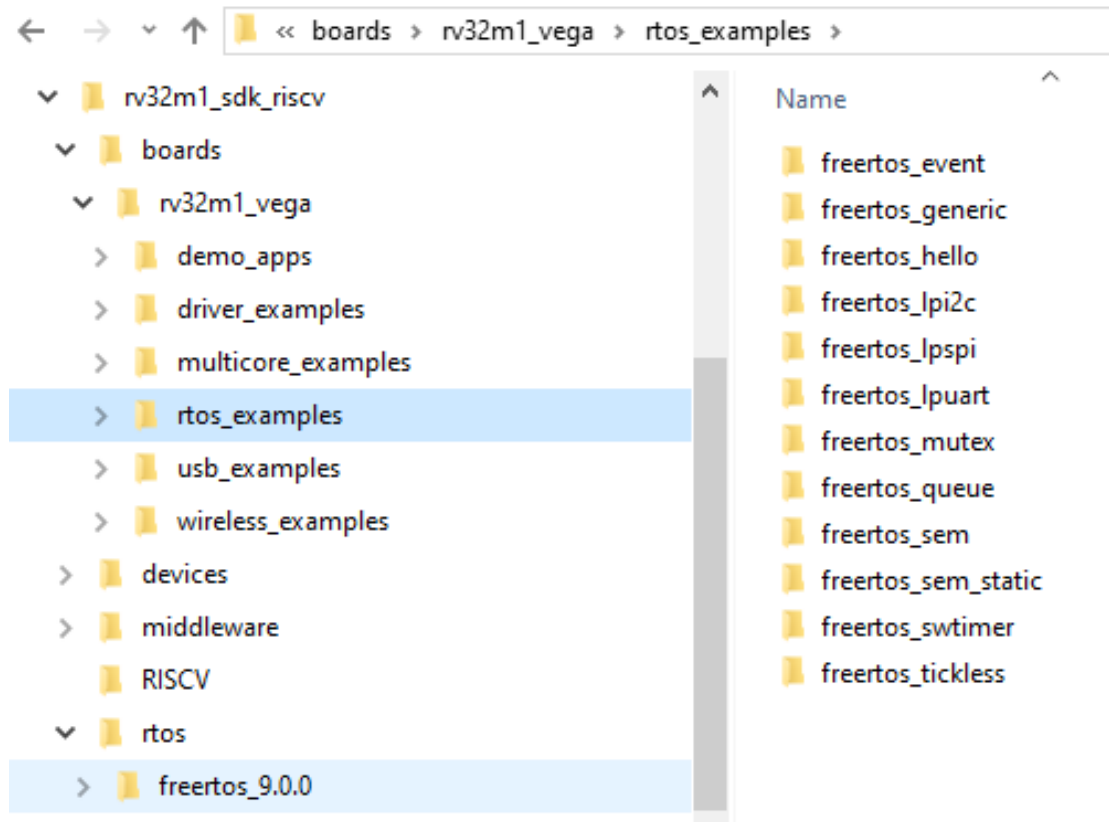


IAR Embedded Workbench



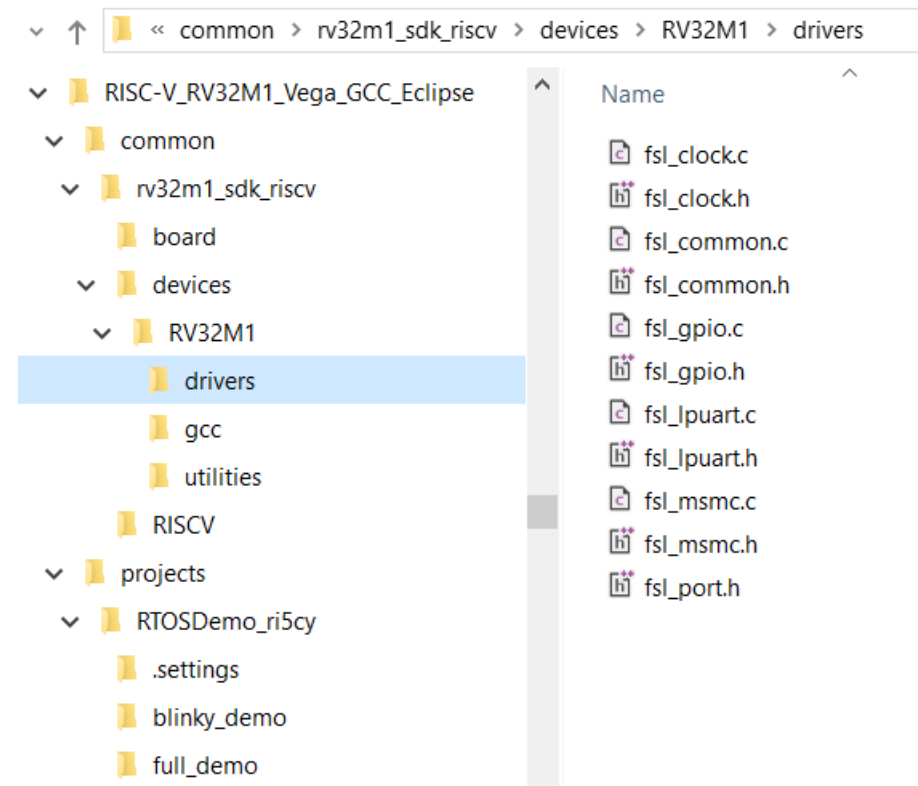
- LLVM for RISC-V is not as good as GCC, and far behind LLVM for Arm
 - Not well optimized for either footprint or performance
 - NXP is working on the enhancement for LLVM for RISC-V, and will contribute back to the community once this task is done.
 - Code size optimizations:
 - Abstracted prologue / epilogue and common code extractions
 - Full support for compressed extension
 - Performance optimizations:
 - Instruction scheduling

FreeRTOS



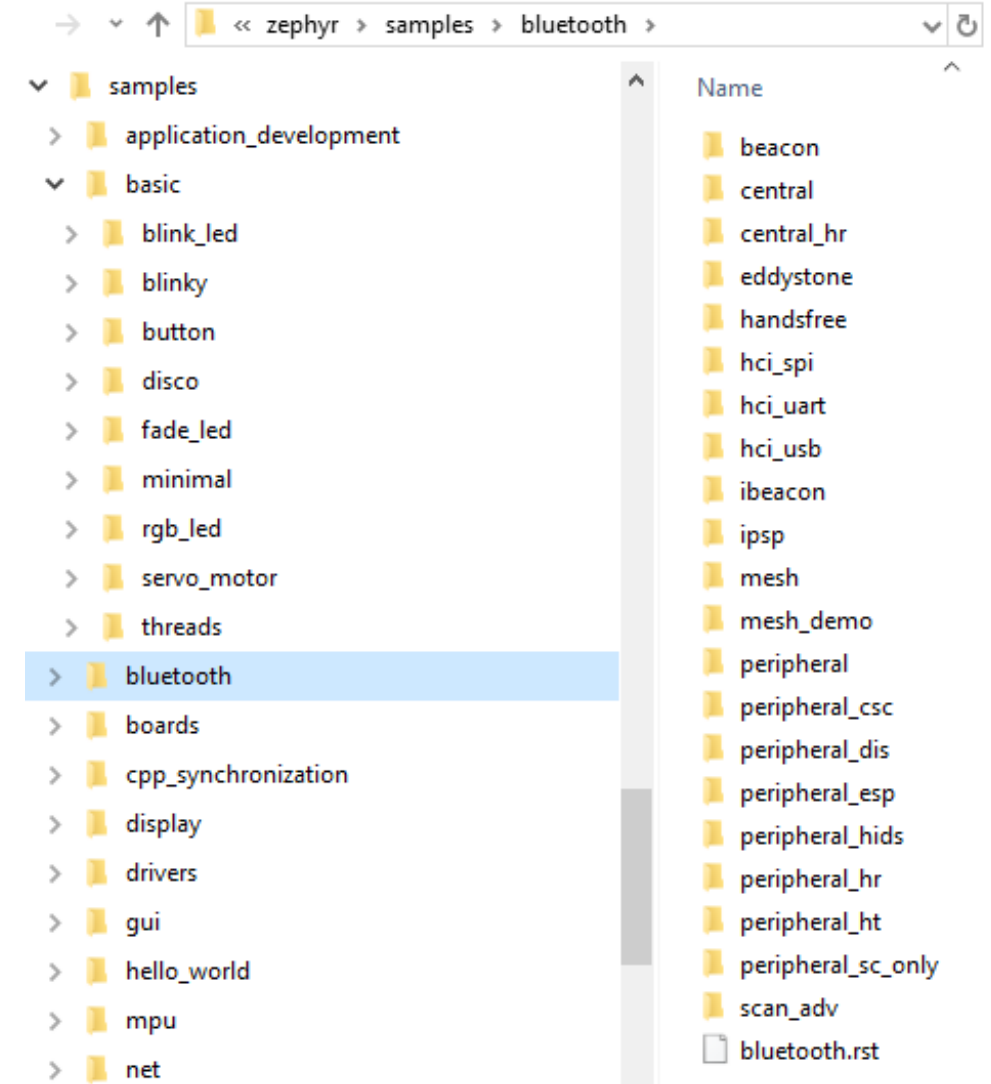
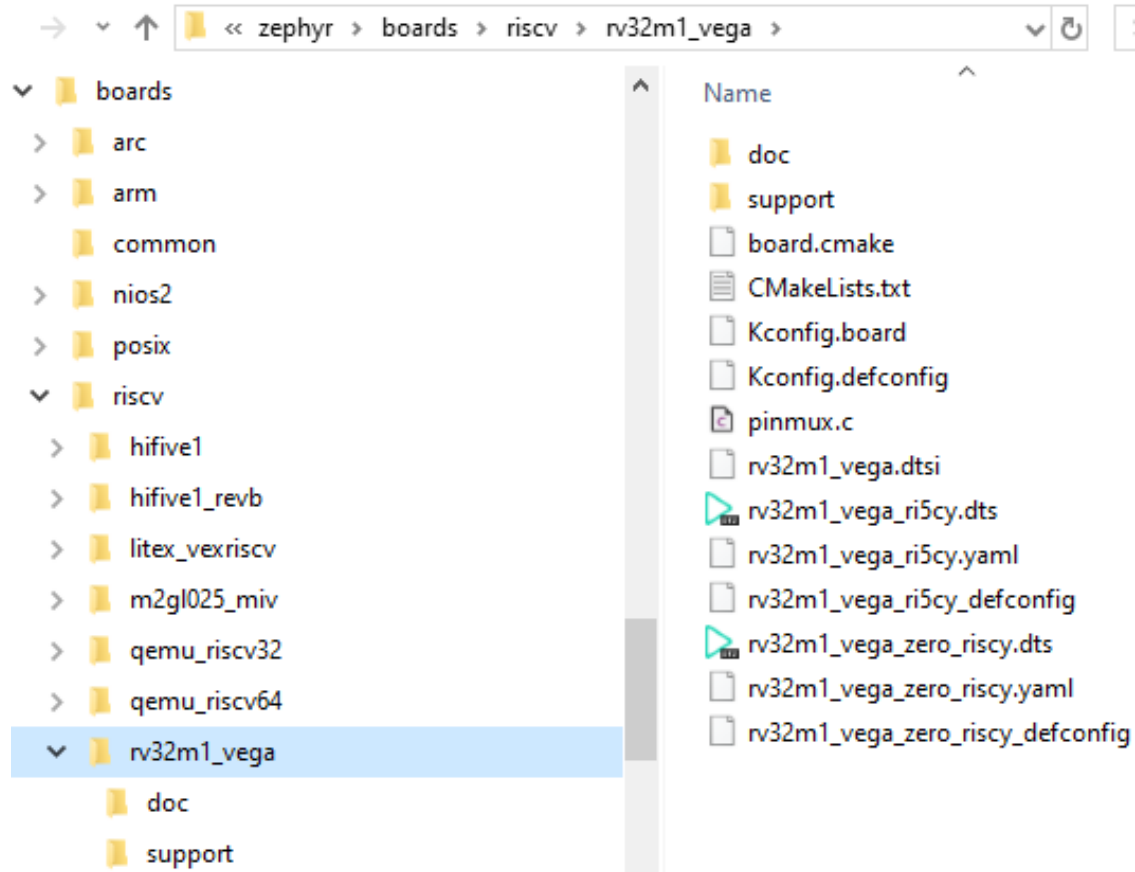
FreeRTOS v9 supported in VEGAboard SDK

<https://github.com/open-isa-org/open-isa.org/releases/>



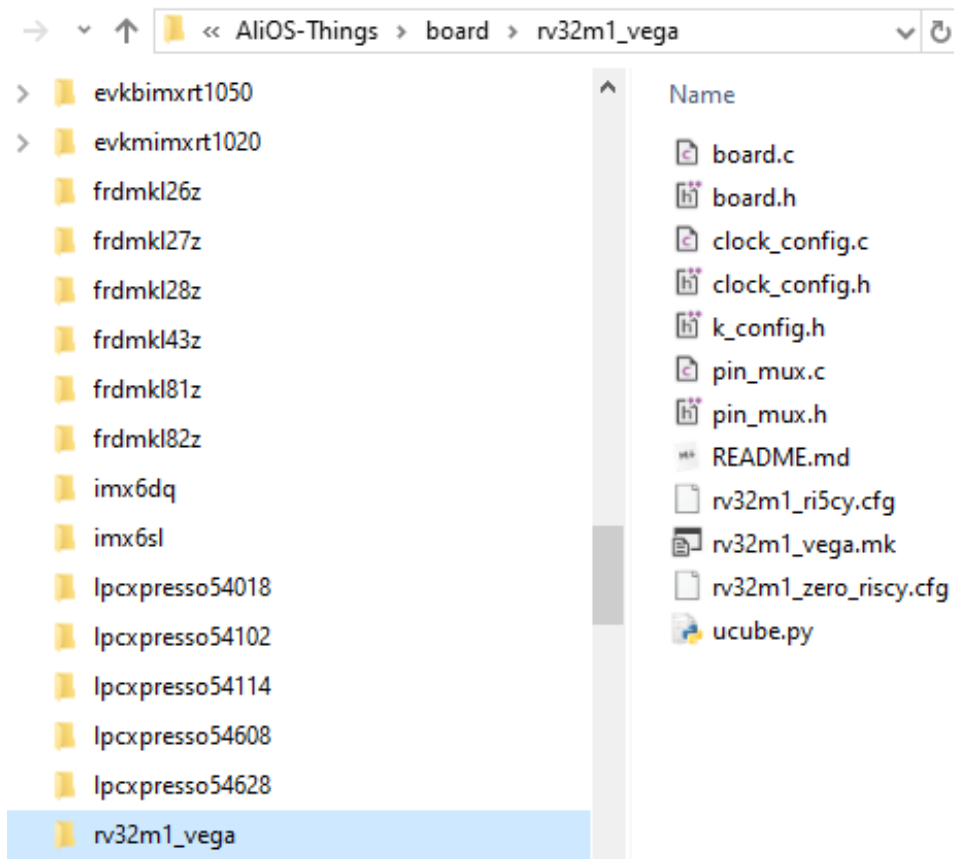
Richard Barry supported VEGAboard in FreeRTOS v10

<https://sourceforge.net/p/freertos/code/HEAD/tree/trunk/>



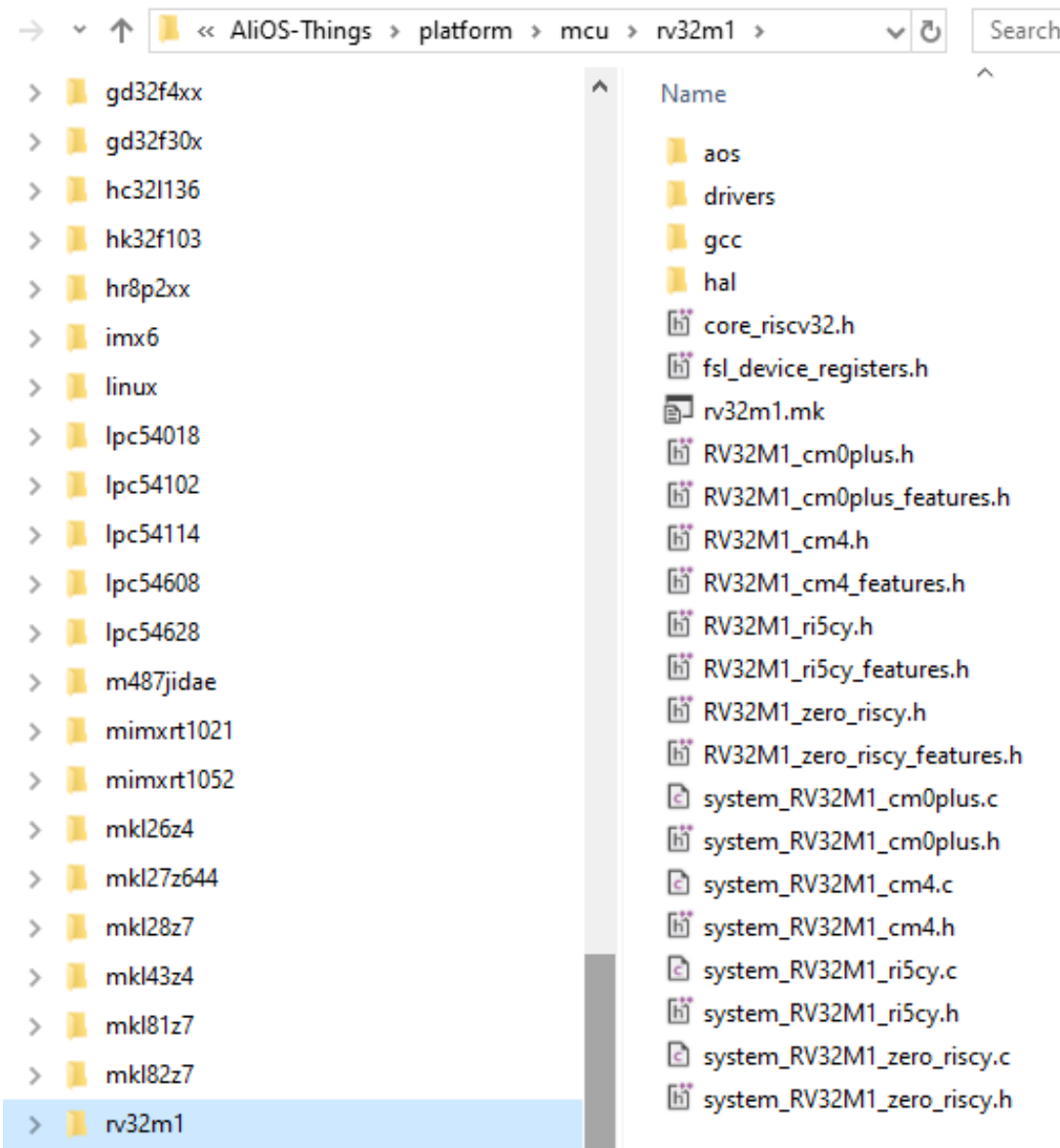
VEGAboard supported in Zephyr

<https://github.com/zephyrproject-rtos/zephyr>

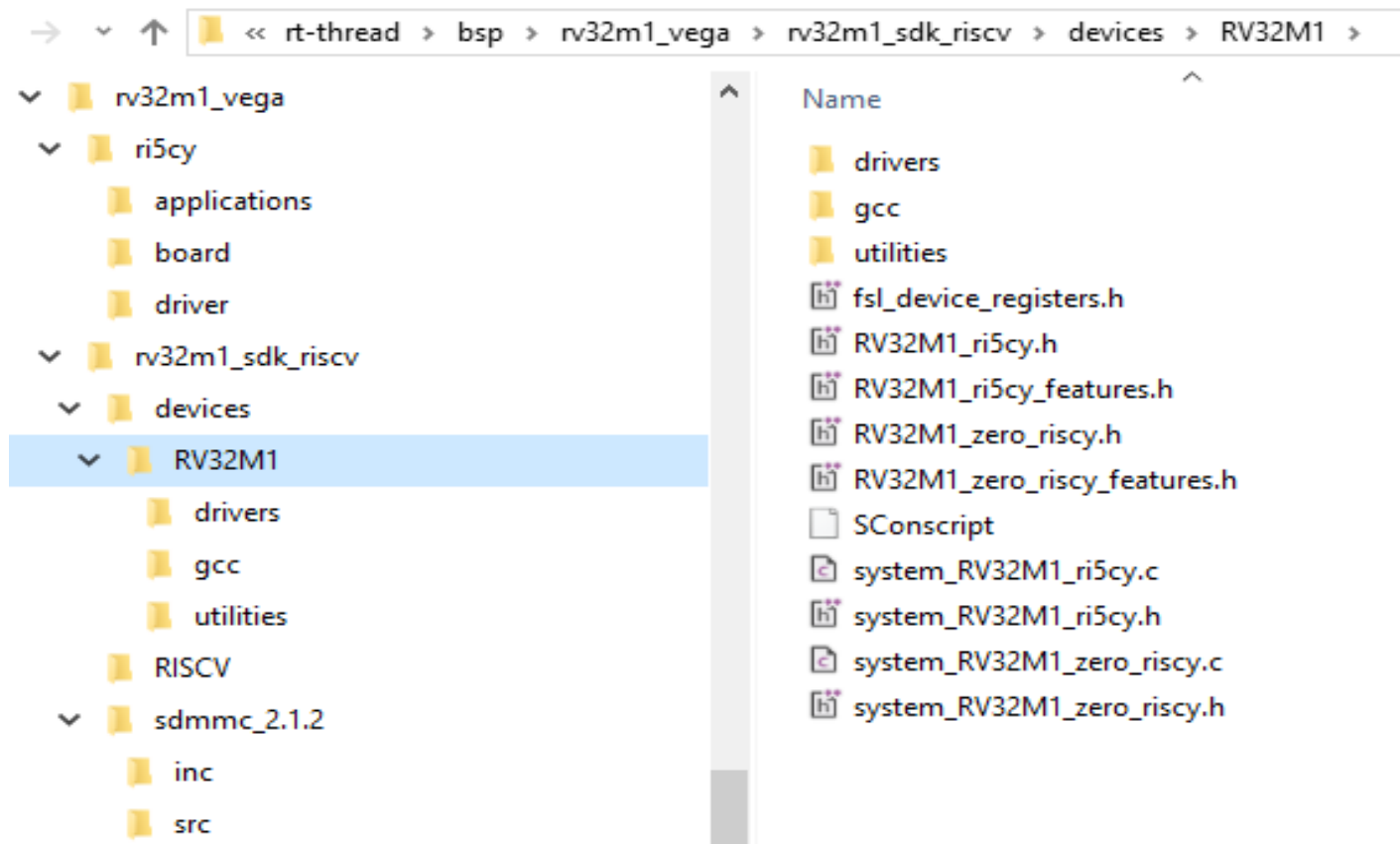


VEGAboard supported in AliOS Things

<https://github.com/alibaba/AliOS-Things>



RT-Thread



VEGAboard supported in RT-Thread

<https://github.com/RT-Thread/rt-thread>

OSDForum 2019

- 100 VEGAboards were used for this forum
- Introduction on RV32M1, VEGAboard and SDK
- 2 hands on sessions
 - SDK + IoT wireless connectivity using the Vega board
 - Zephyr + MicroPython on the Vega board
- Slides and video can be found here
<https://www.osdforum.org/>
- We also worked with partners to create a virtual machine file with toolchain / Eclipse IDE / SDK / Zephyr installed, as well as the instructions
https://github.com/openhwgroup/riscv_vm



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ABOUT OSDFORUM

The Open Source Developer Forum is a workshop that brings open source SW and HW (chips, boards and systems) developers together to collaborate and learn. The OSDForum includes talks from leading industry and academic experts focused on IoT, Edge and Machine Learning development leveraging open source SW and HW building blocks. The agenda also includes a hands on bring up session using a RISC-V based development board that attendees can keep. Made possible by the generous support of our sponsors, the OSDForum is a non-profit event with low attendee fees of \$50 for industry attendees and \$25 for academic attendees (includes the full day of talks, breaks, lunch and a RISC-V development board).

Registration is limited, so don't delay - register today!

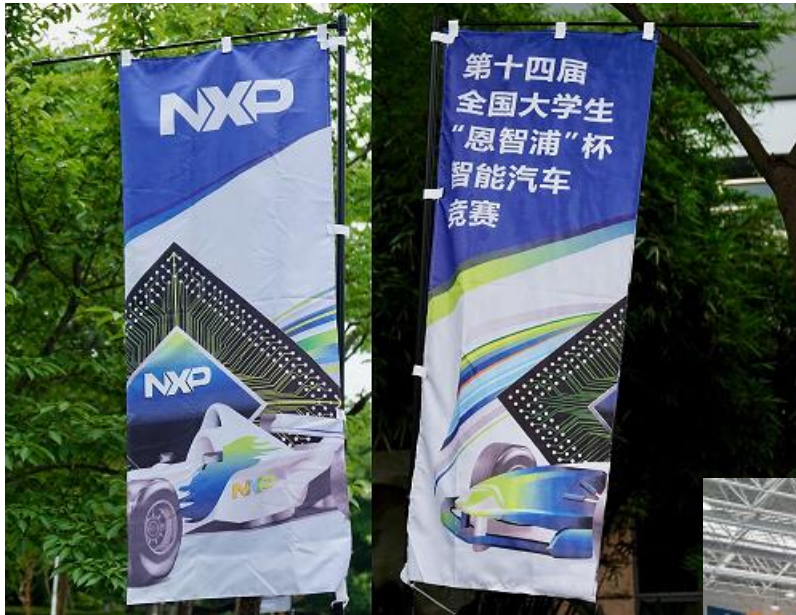
The OSDForum is co-hosted by CMC Microsystem, the Eclipse Foundation and the OpenHW Group.



RISC-V dev board attendees will keep

Support NXP CUP Smart Car Competition in China

- 3rd Partner designed core board with RV32M1 SOC for University teams selection



RISC-V Design Contest in China

- RISC-V is not only an open ISA, but also an open ecosystem for designers and SW developers
- Aims to promote the awareness and use of RISC-V in China through this contest
- Encourage practical design works to enrich the entire community resources

Status

- Applicants : 69
- Passed : 40
- Application Projects including
 - 使用Rust语言开发运行于Vega-Lite开发板的RISC-V程序
 - LiteOS移植
 - 移植micro-ROS 的操作系统部分 (RTOS NuttX)
 - 移植uclinux至织女星开发板
 - 基于RV32M1的专业阿卡贝拉创作平台
 - 基于micropython的BLE协议栈在RISC-V上的实践
 - 基于织女星开发板的太阳能电池板控制器的设计
 - CAN协议转蓝牙转换器
 - 基于RV21M1和SDK的便携式近红外光谱分析仪原形设计
 - ...

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Open-ISA



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Directed By

中国RISC-V产业联盟 (CRVIC)



University Programs and Partnership

- University Course
 - VEGAboard has been used in Tianjin University for course
 - Outcome: Experimental reports on RT-Thread application development on VEGAboard
 - Joint-Lab
 - Books
 - Research Project
 - Tools
 - Software
-
- Welcome University, Institute, Tool vendors, Software Company for further cooperation...





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