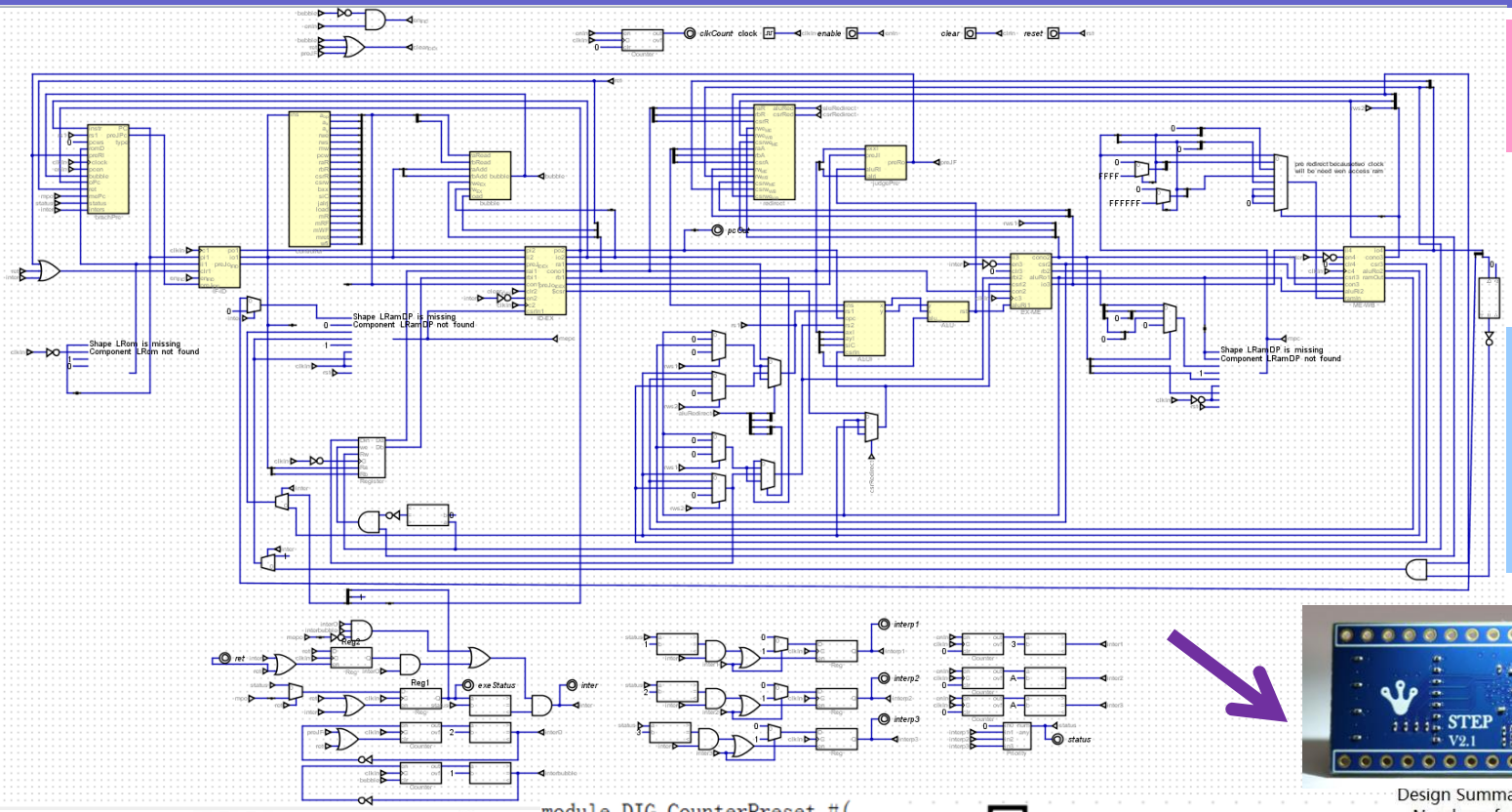
RISC-V graphic program design(Non-program)

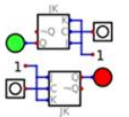


EDA must be Agile Design

HDL/Chisel Not Easy

***Digiblock*: Like "Scratch" Built by block ->Verilog code**

Digiblock
Logic Designer and Simulator



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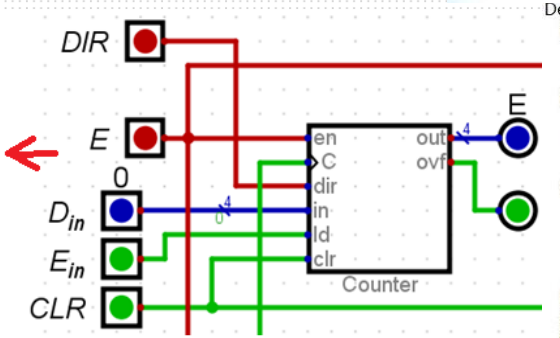
```
module DIG_CounterPreset #(
    parameter Bits = 2,
    parameter maxValue = 4


input C   ,
input en ,
input clr,
input dir,
    input ld ,
input [(Bits-1):0] in  ,
output [(Bits-1):0] out,
output ovf
);
```



Design Summary:

Number of registers:	635 out of 4635 (14%)
PFU registers:	635 out of 4320 (15%)
PIO registers:	0 out of 315 (0%)
Number of SLICEs:	1040 out of 2160 (48%)
SLICEs as Logic/ROM:	1040 out of 2160 (48%)
SLICEs as RAM:	0 out of 1620 (0%)
SLICEs as Carry:	130 out of 2160 (6%)
Number of LUT4s:	2075 out of 4320 (48%)
Number used as logic LUTs:	1815
Number used as distributed RAM:	0
Number used as ripple logic:	260
Number used as shift registers:	0

Number of PIO sites used: 28 + 4(JTAG) out of 105 (30%)
Number of block RAMs: 10 out of 10 (100%)
Number of GSRs: 0 out of 1 (0%)