RISC-V® Architecture and RISC-V® International Open Source (RIOS) Laboratory at Tsinghua-Berkeley Shenzhen Institute

November 2019
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University of California, Berkeley

@risc_v

RIOS (“Ree-Oss”) Laboratory at Tsinghua-Berkeley Shenzhen Institute (TBSI)

- RIOS: RISC-V International Open Source Laboratory
  - 5-year mission to help raise the RISC-V ecosystem to the state-of-the-art (“uncore” IP)
  - A nonprofit organization that measures success by technology transfer
  - Produce industrial strength IP protected against patent lawsuits
- TBSI: Tsinghua-Berkeley Shenzhen Institute
  - Tsinghua University and UC Berkeley joint venture located in Shenzhen established 2014
  - Teach RISC-V, open source grad courses at TBSI to create future leaders of technology
- RIOS Director: UC Berkeley Professor David Patterson in Berkeley
- Co-Director: Dr. Zhangxi Tan in Shenzhen (Berkeley and Tsinghua alumnus)
- Co-Director: Tsinghua Professor Lin Zhang in Shenzhen
- Distributed lab with majority of engineers at TBSI
- Base funding by Shenzhen Municipality + matching funds from companies and donors + loaning engineers to work on open source projects
  - Imagination and Western Digital have already expressed interest

My Five-Year Projects

Find leaders from multiple disciplines interested in new direction

Spend 1 year coming up with vision

Hold 2 retreats/year with visitors

Mid-course correction 2.5 years

Celebrate end of project after 5 years

Years	*Project Title (Impact)*	*Faculty Director, PIs* ***(NAE in Bold)***	*Students (ACM fellows)*
1977-1981	X-Tree: A Tree-Structured Multiprocessor	Despain, **Patterson**, Sequin	12 (2)
1980-1984	Reduced Instruction Set Computer *(RISC-I, RISC-II)*	**Patterson, Ousterhout**, Sequin	17 (1)
1983-1986	SOAR: Smalltalk On A RISC aka "RISC-III" (*Generational Garbage Collection*)	**Patterson, Ousterhout**	22 (1)
1985-1989	SPUR: Symbolic Processing Using RISCs aka "RISC-IV" (*Snoopy bus protocols*)	**Patterson**, Fateman, Hilfinger, **Hodges**, **Katz**, **Ousterhout**	21 (4)
1988-1992	RAID: Redundant Array of Inexpensive Disks *(RAID-I, RAID-II)*	**Katz**, **Ousterhout**, **Patterson**, **Stonebraker**	16 (4)
1993-1998	NOW: Network of Workstations *(Inktomi, Internet Clusters)*	**Culler**, **Anderson**, **Brewer**, **Patterson**	25 (4)
1997-2002	IRAM: Intelligent RAM (*Processor in Memory*)	**Patterson**, Kubiatowicz, Wawrzynek, **Yelick**	12 (2)
2001-2005	ROC: Recovery Oriented Computing Systems (*Crash-only software, Microreboot*)	**Patterson**, Fox	11
2005-2011	RAD Lab: Reliable Adaptive Distributed Computing Lab *(Spark, Mesos)*	**Patterson**, Fox, **Jordan**, Joseph, **Katz**, **Shenker**, Stoica	45
2007-2013	Par Lab: Parallel Computing Lab *(Communication Avoiding Algorithms, RISC-V)*	**Patterson**, Asanovic, **Demmel**, Fox, Keutzer, Kubiatowicz, Sen, **Yelick**	36
2011-2016	AMPLab: Algorithms, Machines, & People	Franklin, **Jordan**, Joseph, **Katz**, **Patterson**, **Shenker**, Stoica	34
2012-2017	ASPIRE Lab: Algorithms and Specializers for Provably optimal Implementations with Resilience and Efficiency	Asanovic, Alon, Bachrach, **Demmel**, Fox, Keutzer, Nikolic, **Patterson**, Sen, Wawrzynek	31
2017-2022	RISELab: Real-time Intelligent Secure Explainable systems	Stoica, Gonzalez, Hellerstein, Popa, **Jordan**, **Patterson**, **Katz**	≈35

David Patterson, "How to build a bad research center," *Communications of the ACM*, 57.3 (2014): 33-36.

31 (12 NAE of 16 total NAE in CS) **317 (18 ACM)**

Berkeley Style Retreats

- Been doing retreats for 30+ years (RISC, RAID, Network of Workstations, ParLab, …)
- Held twice a year for 5 years of project
- 3 day offsite meeting
- All students, staff, and faculty from research project
  - Plus visitors from sponsoring organizations
  - As many visitors as people in the project
- Format
  - Talks during the day
  - Directed discussions over meals
  - Poster sessions in the evenings
  - Informal break afternoon of second day
- Last session is feedback from visitors
- Lots of guidance over time from outsiders (vs paper reviewers)

Berkeley Research Retreat Benefits

- Creates 2 deadlines / year
- Students practice giving talks
- **Key piece is feedback at end**
  - Can't argue with feedback
- Helps with technology transfer
- Enhances group's reputation
- Builds team spirit (all work & play together)
- Always amazed of value after its over

Most important technique to help run project/center with several faculty and many grad students

Patterson, D.A., 2014. How to build a bad research center. *Communications ACM*, *57*(3), pp.33-36.

RISC-V Origin Story

- UC Berkeley Research using x86 & ARM?
  - Impossible – too complex *and* IP issues
- 2010 started "3-month project" to develop own clean-slate ISA
  - Krste Asanovic, Andrew Waterman, Yunsup Lee, Dave Patterson
- 4 years later, released frozen base user spec

Why are outsiders complaining about changes of RISC-V in Berkeley classes?

What's Different About RISC-V?
("RISC Five", fifth UC Berkeley RISC)

- Free and Open
  - Anyone can use
  - More competition ⇒ More innovation
  - Pick ISA, then vendor

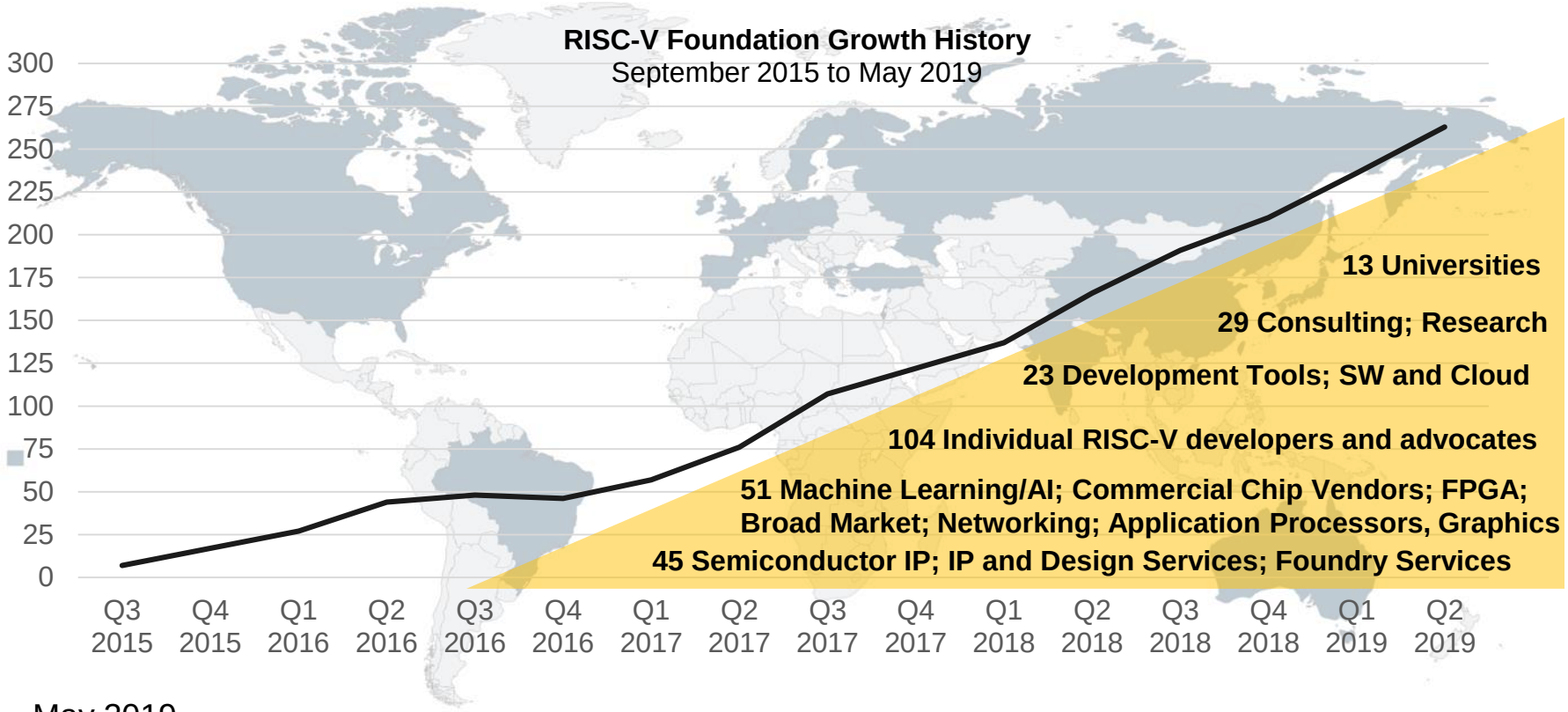
- For Cloud & Edge
  - From large to tiny computers
- Secure/Trustworthy
  - Design own secure core
  - Open cores ⇒ no secrets

- Simple, Elegant, Modular
  - 25 years later, learn from 1st gen RISCs
  - Far simpler than ARM and x86
  - **Can add custom instructions**
  - **Input from software/architecture experts BEFORE finalize ISA**
- Community evolves
  - RISC-V Foundation owns RISC-V ISA

RISC-V in the News

- 3 articles in *The Economist*, October 5, 2019. "Open Season", "Fab in India", "Your own RISC"
- *"[Open source software] has been a striking success. … Now the model is spreading to chips. RISC-V is a set of open source designs for microchips developed a decade ago at the University of California, Berkeley. ... These moves are welcome for two reasons.*
- *"The first is economic. RISC-V competes with closed-source designs from ARM … A dose of competition could lower prices.*
- *"The second is geopolitical. … [A tech cold war] threatens to damage a computer industry that has become thoroughly globalised. ... A complete rupture would be extraordinarily costly… Open-source computing can help calm tempers. That would be good for everyone."*

More than 300 RISC-V Members in 28 Countries Around the World

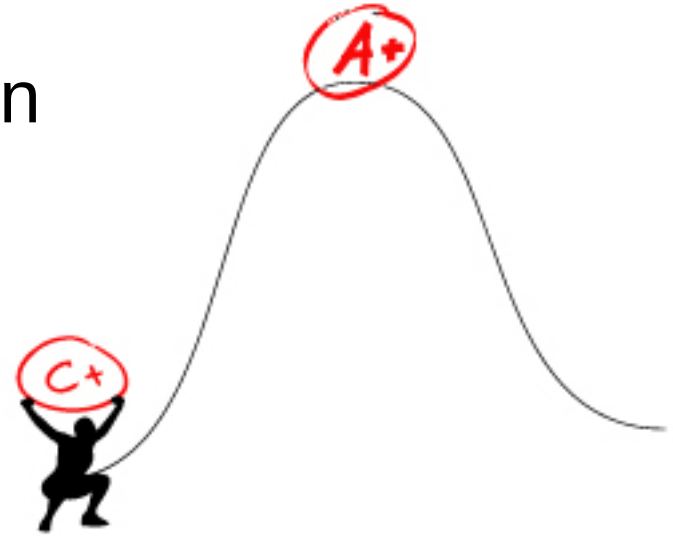


May 2019


SEMICONDUCTOR IP
IP AND DESIGN SERVICES
FOUNDRY SERVICES
CONSULTING/RESEARCH
DEVELOPMENT TOOLS
SW AND CLOUD
MACHINE LEARNING/AI
COMMERCIAL CHIP VENDORS
FPGA
NETWORKING
BROAD MARKET
APPLICATION PROCESSORS, GRAPHICS
RISC-V

Computer Architecture Evaluation

- Architect's target: max performance, min cost for a workload
- Architects grade "on a curve", not "absolute scale"
- Computers of same era have same about technological options, so which has best cost-performance?
- Need fair comparison for Internet of Things, likely first market for RISC-V



State of Benchmarks for IoT/Embedded Computers

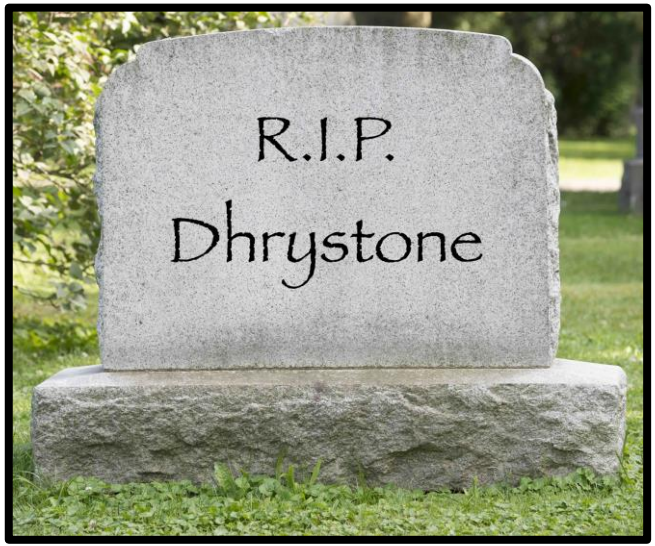
- Billions of Internet of Things (IoT) devices shipped soon
- Still no high quality, widely reported benchmark for embedded computers

Yunsup Lee, SiFive CTO, Keynote address "Opportunities and Challenges of Building Silicon in the Cloud" 12/5/18 RISC-V Summit:

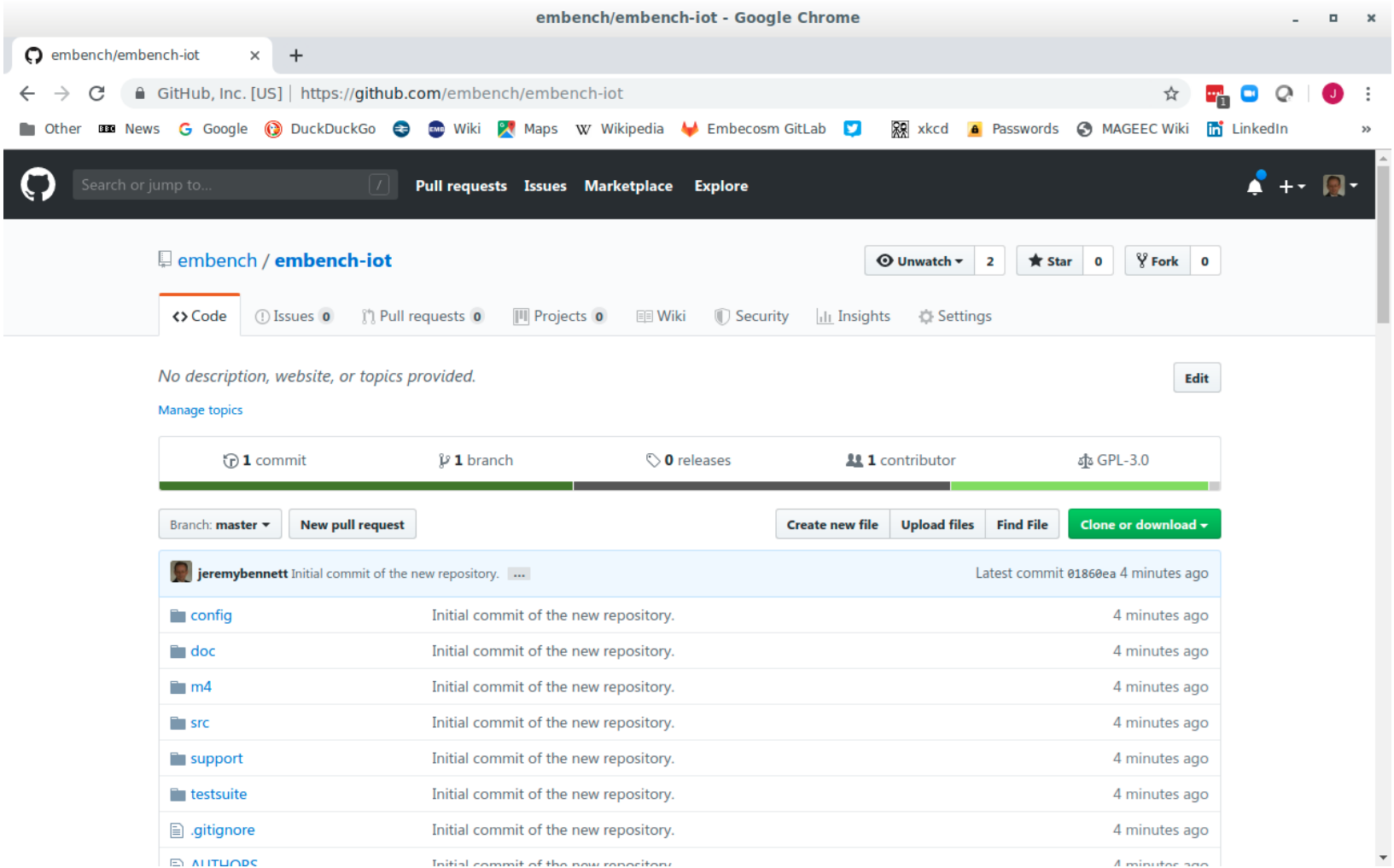
"*... the benchmark scores are 4.9 CoreMarks/MHz and 2.5 DMIPS/MHz. I'm saying this in front of Dave [Patterson], who doesn't really like Dhrystone or CoreMark as benchmarks. Sorry. This is the industry standard benchmark I learned*."

It's past time to apologize; let's fix!

Embench



- Group from academia and industry develop
- Free
- Easy to Port
- Suite of 20 Real Programs (vs 1 Synthetic Program)
- Geometric Mean & Geometric Standard Deviation of Ratios to Reference Platform
- Also Report Code Size, Context Switch Time, and Interrupt Latency
  - Necessary for embedded IoT devices yet novel part of formal benchmark
- Sustaining Organization involving Academia and Industry to Evolve over Time
- Follows Agile Benchmark Development Philosophy: Versions 0.5, 0.6, …
- Given current state of widely reported benchmarks for embedded computing, we believe Embench—even the 0.5 version—will be a big help to the IoT field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Branch: master New pull request
Create new file Upload files Find File Clone or download
jeremybennett Initial commit of the new repository.
Latest commit 01860ea 4 minutes ago
config Initial commit of the new repository. 4 minutes ago
doc Initial commit of the new repository. 4 minutes ago
m4 Initial commit of the new repository. 4 minutes ago
src Initial commit of the new repository. 4 minutes ago
support Initial commit of the new repository. 4 minutes ago
testsuite Initial commit of the new repository. 4 minutes ago
.gitignore Initial commit of the new repository. 4 minutes ago

Call for Participation (info@embench.org)

- After good start, need and want help to complete version 0.5 (like MLPerf)
- We hold monthly meetings (including remote participants)
- Hope Embench 0.5 finalized in time to begin collecting and reporting results before the end of the year (like MLPerf did)
- If you have the time and interest in helping, please send email to info@embench.org

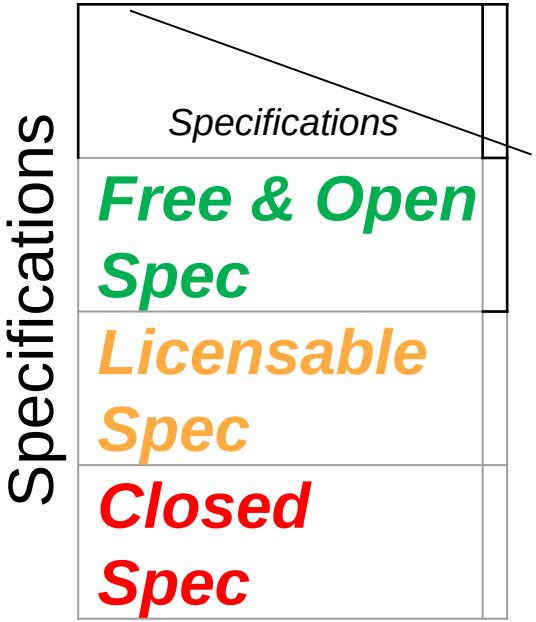
Free & Open Instruction Set (ISA) vs Free & Open Source Hardware?

- Specifications
  - Instruction Set Architecture (for example, RISC-V)
  - Similar to Portable Operating System Interface (POSIX) standard in software
- Designs (“source code”)
  - RISC-V Rocket
  - Similar to Linux in software
- Products
  - OURS Pygmy chip
  - Similar to RedHat 7.5 in software

3 Types of Specifications or Designs

1. Free & Open
   - No fee, anyone can use
   - Can design it yourself, share with others, get from others
2. Licensable
   - Company owns, pay fee to use
   - Can’t share with or get from others
3. Closed
   - Company owns, others cannot use

Need Free & Open Specification To Have Free & Open Designs



Need Free & Open Specification To Have Free & Open Designs

Designs ("Source")

Products

Specifications

Designs / Specifications	***Free & Open Designs***	***Licensable Designs***	***Closed Designs***	
Free & Open Spec				
Licensable Spec				
Closed Spec				

Need Free & Open Specification To Have Free & Open Designs

Designs ("Source")

Products

Specifications

Specifications \ Designs	***Free & Open Designs***	***Licensable Designs***	***Closed Designs***	
Free & Open Spec				
Licensable Spec				
Closed Spec				Based on Closed Designs

Need Free & Open Specification To Have Free & Open Designs

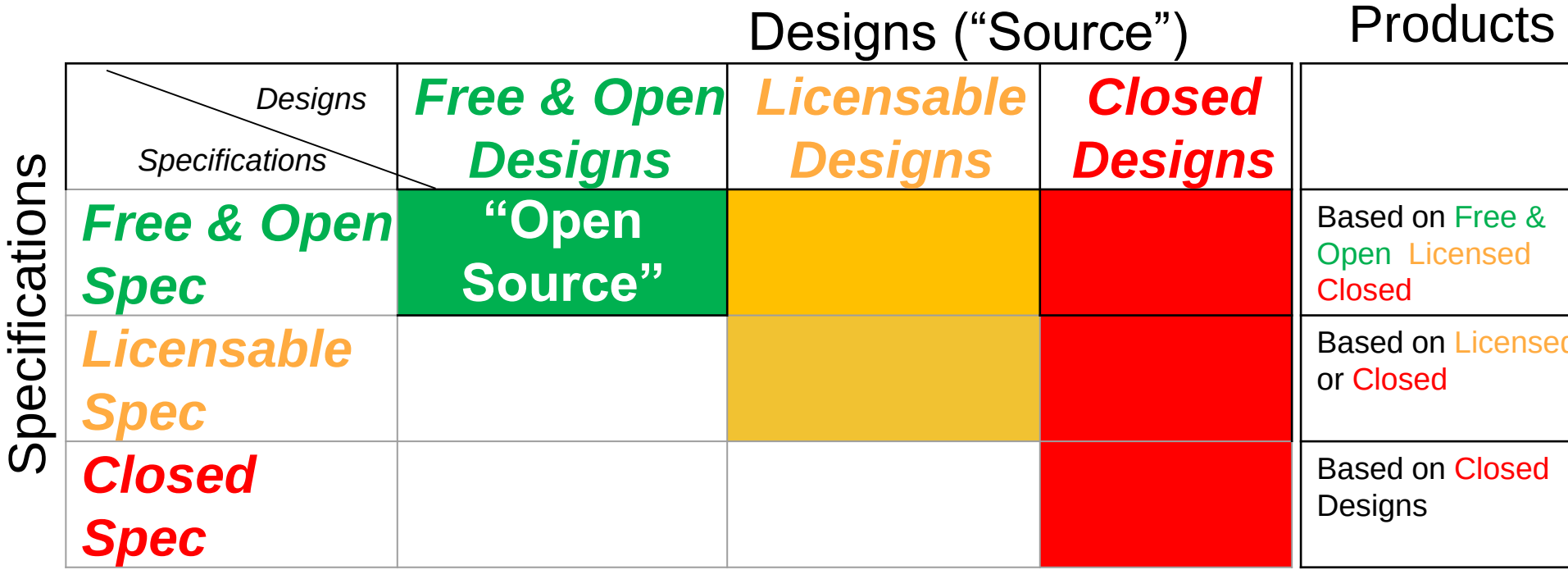
Designs ("Source")

Products

Specifications

Specifications \ Designs	Free & Open Designs	Licensable Designs	Closed Designs	
Free & Open Spec				
Licensable Spec		$5M + 4%	$25M	Based on Licensed or Closed
Closed Spec				Based on Closed Designs

Need Free & Open Specification To Have Free & Open Designs



Number of Open Source, Licensable, Closed Designs

Designs (“Source”)

Specifications \ Designs	Free & Open Designs	Licensable Designs	Closed Designs
RISC-V (Open)	≈25	≈50	≈25
ARM (Licensable)	0	≈20	≈25
x86 (Closed)	0	0	≈15

Products

Based on Free & Open Licensed Closed
Based on Licensed or Closed
Based on Closed Designs

More RISC-V Designs than any other ISA?

- Foundation list of licensable and open source RISC-V cores

Processor Name	*Developer*	*Processor Name*	*Developer*
Ariane	ETH Zurich, Università di Bologna	ReonV	Lucas Castro
Berkeley Out-of-Order Machine (BOOM)	UC Berkeley, Esperanto	Reve-R	Gavin Stark
DarkRISCV	Darklife	RI5CY	ETH Zurich, Università di Bologna
freedom	SiFive	Riscy Processors	MIT
Hummingbird E200	Bob Hu	RiscyOO	MIT
Ibex	lowRISC	Roa Logic RV12	Roa Logic
Instant SoC	FPGA Cores	rocket	UC Berkeley, SiFive
Lizard	Cornell	RPU	Domipheus Labs
Maestro	João Chrisóstomo	SCR1	ETH Zurich, Università di Bologna
Minerva	LambdaConcept	SERV	Olof Kindgren
MR1	Tom Verbeure	Shakti	IIT Madras
OPenV/mriscv	OnChipUIS	SweRV EH1	Western Digital Corporation
ORCA	VectorBlox	VexRiscv	SpinalHDL
PicoRV32	Clifford Wolf		

Why so many processors?

- Fun part of computer to design and improve
- Engineers like making faster car by improving engine
- But more to car than only the engine
  - Streering Wheel
  - Pedals
  - Fuel tank
  - Fuel gauge
  - Speedometer
  - Mirrors
  - Headlights
  - Turn signals
  - Taillights
  - …

Need more than processor to build a system

- Large costs to license other IP as of 2016*
- Cost increasing with newer technology

Semiconductor Technology Node	*40 nm*	*28 nm*	*16 nm*	*12 nm*	*7 nm*
DRAM Controller	$125,000	$125,000	$125,000	?	?
DRAM Phy (physical interface)	$280,000	$390,000	$750,000	?	?
PCI-E Controller	$125,000	$125,000	$125,000	?	?
PCI-E Phy (physical interface)	$375,000	$510,000	$775,000	?	?
Phase Lock Loop	$50,000	$35,000	$50,000	?	?
Low Voltage Differential Signaling IO	$36,000	$40,000	$200,000	?	?

*Khazraee, M., Zhang, L., Vega, L. and Taylor, M.B., 2017, April. Moonwalk: NRE optimization in ASIC clouds *ASPLOS Conference*.

Open Source Analog IP like Phy?

- Prof. Mark Horowtiz, Stanford University

"I don't think the issue is technical difficulty, since Phys exist. I think the question is economic. Open source donates the NRE cost of an object. This is done to lower the cost of an essential, but non differentiating, part of the system and/or lower its maintenance costs. It also assumes that the deployment cost is zero."

"Phys current costs are recoup NRE, and to pay for the support (help to ensure Phy works in your environment: packaging, board, power distribution) and debug the design when it comes out (to demonstrate it isn't the Phy's problem). The harder problem is to pay for the recurring engineering support needed for each deployment. While you might argue it is not strictly needed, I don't think anyone is going to risk their chip design on an untested Phy."

Patent Trolls Attack Open Source IP blocks?

- Troll: Company without products that uses patents as legal weapons
  - “Non-Practicing Entities” (NPE)
  - Often buy patents from failing companies
- Unfortunately US Patent Office issues vague patents, and may not novel idea
- Troll sends threatening letters to small companies, asking tens to hundreds of thousands of dollars in licensing fees
  - 40% companies in lawsuits with trolls report significant operational impact
- Many pay even if they don’t infringe since litigation can costs millions of dollars and can take years of court battles
  - Faster and easier to settle

Patent Threat to Open IP Blocks?

- Consulted Prof. Jennifer Urban and Prof. Erik Stallman of UC Berkeley Law School on IP blocks, patents, and licenses
  - Open source hardware IP blocks is a new area for US law
  - Starting from old patents and papers a good idea, but others can file improvement on expired patent to get a new patent
- Legal concept of preventing patent infringement by searching in beforehand: “Freedom to Operate” patent search
  - Best performed by law firms experienced in hardware patents (costs >$10,000, <$100,000)
- Profs Urban and Stallman suspect licenses like BSD (“Berkeley Software Distribution”) right for software but wrong for hardware
  - They and their students interested in working on problem and may propose good license for IP blocks in 6-9 months

RIOS (“Ree-Oss”) Laboratory at TBSI

- RIOS: RISC-V International Open Source Lab
  - 5-year mission to improve the RISC-V ecosystem (“uncore”)
  - A nonprofit organization measures success by tech transfer
  - Produce industrial strength IP protected against patent trolls
  - Funding from Shenzhen Municipality and industry collaborators
- Rios is Spanish for “rivers”
  - River name symbolizes collection of resources from many lands to create a strong force that changes the landscape
  - Like RIOS lab at TBSI will do for RISC-V and information technology landscapes