



# CHINA FORUM 2019

CALISTA REDMOND  
CEO, RISC-V FOUNDATION

 @CALISTA\_REDMOND



# Thank you!



**Dr. Zhuangxi Tan**

Conference Chair

Vice Managing Director of  
RIOS (RISC-V International  
Open Source Labs)



**Prof. Yungong Bao**

Program Committee  
Chair

中国开放指令生态 RISC-  
V 联盟 CRVA Alliance

ICT (Institute of  
Computing Technology)  
at CAS



**Jesse Fang**

Steering Committee Chair

Leader RISC-V  
Foundation China  
Committee



**Dr. David Patterson**

RISC-V International Open  
Source Laboratory (RIOS  
Laboratory)



**Dr. Wayne Dai**

Chairman, 中国RISC-V产业  
联盟 CRVIC

CEO VeriSilicon Holdings

**TBSI** 清华-伯克利深圳学院  
Tsinghua-Berkeley Shenzhen Institute



2019  
China Forum  
Sponsors



## 1980s

Battle of unique, special-purpose and simple general-purpose chips. Rise of Intel x86 CISC chips for general purpose and slower adoption of RISC chips.

Drawbacks of patent license costs with high barriers to entry



## 1990s

CPU lifecycle shrinks from years to months, as performance demands accelerate. Moore's law often cited to double transistors every 12-18 months relative to cost.

Computing needs diverged across implementations, from servers to cars. ARM grows in embedded.



## 2000s

Performance is critical as physical limits are in sight, age of accelerators and io innovation.

Mobile drives innovation.

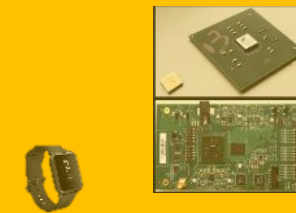
Grass roots of open cores such as OpenRISC and OpenSPARC.



## Today

Exponential growth from diverse computing need, solved by custom processor development + stakeholder collaboration.

Low barriers to entry with open processor IP. RISC-V specification is free and open.



# Evolution of the processor industry



## Cloud and data center applications

top cloud providers like Amazon and Alibaba are designing their own chips.



## Mobile and wireless

continue rapid evolution with each generation of hardware and increased capability.



## Automotive

 is

transforming from autonomous vehicles to infotainment to safety, the whole vehicle relies on innovative electronics.



## Consumer and IoT devices

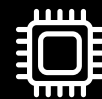
 bring incredible

innovation and volume with billions of connected devices being in the next 5-10 years.



## Industrial IoT

incorporating artificial intelligence in manufacturing and industrial processes.



**Memory** was the largest semiconductor category by sales with \$158 billion in 2018, and the fastest-growing, with sales increasing

# Global collaboration

# Global innovation

# A community of many experts and stakeholders



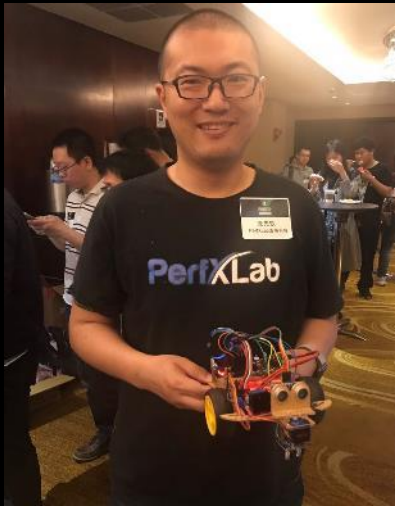
# CHINA

MORE THAN 200 MEMBERS HAVE JOINED THE CRVA AND CRVIC ASSOCIATIONS AS WELL AS 33 MEMBERS IN THE GLOBAL RISC-V FOUNDATION. ACROSS 2019 WE'VE LED DISCUSSIONS IN 6 CITIES AS WELL AS HOSTED A DAY OF TALKS AT THE WORLD INTERNET CONFERENCE. IN NOVEMBER, WE HOSTED 500 ATTENDEES AT THE CHINA RISC-V FORUM.





# Local collaboration ...



China Committee



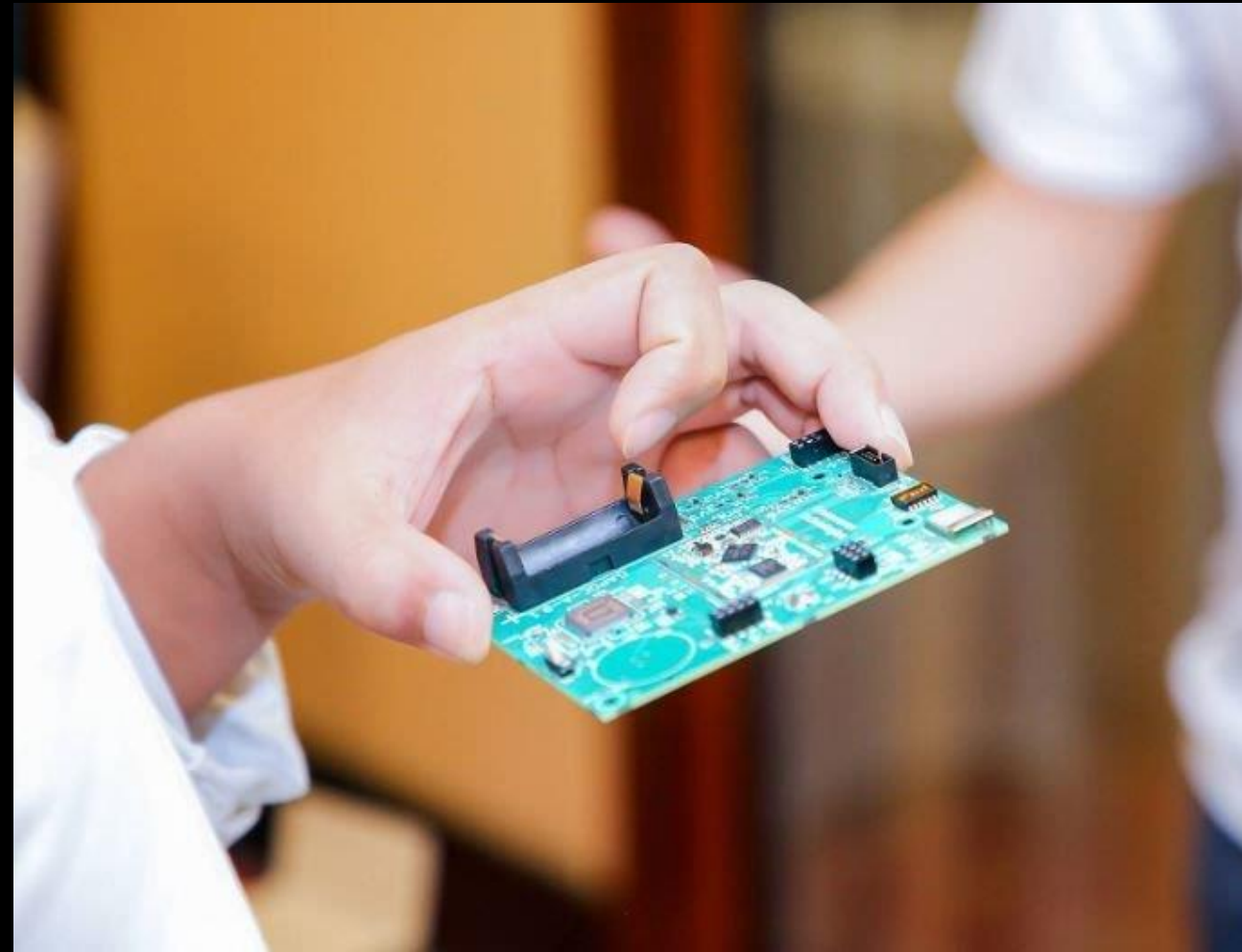
中国开放指令生态 (RISC-V) 联盟  
China RISC-V Alliance



...Global progress

**Global partners and  
supply chain**

**Global opportunity**





# China leadership in global RISC-V revolution



RISC-V International Open Source Laboratory (RIOS Laboratory) RISC-V research at Tsinghua-Berkeley Shenzhen Institute (TBSI) by the University of California at Berkeley and [Tsinghua University](#). June 2019



"Pingtoug said its processor achieves 7.1 Coremark/MHz at a frequency of 2.5GHz on a 12nm process node, which is **40 percent more powerful** than any RISC-V processor produced to date." Nitin Dahad, *EE/Times* July 2019

**Huami's Upcoming Huangshan 1S Processor Said To Be Built On 7nm**  
[Huami](#) is one of the top wearable manufacturers in the world today released its first self-developed RISC-V based Huangshan 1 processor last year August 27, 2019

# Welcome to the RISC-V revolution!



- **RISC-V** is the open-source hardware Instruction Set Architecture (ISA)
- Frozen base user spec released in 2014, contributed, ratified, and openly published by the RISC-V Foundation

**The RISC-V Foundation** is a non-profit entity serving members and the industry

Our mission is to accelerate RISC-V adoption with shared benefit to the entire community of stakeholders.

- ✓ Drive progression of ratified specs, compliance suite, and other technical deliverables
- ✓ **Grow the overall ecosystem / membership**, promoting diversity while preventing fragmentation
- ✓ **Deepen community engagement and visibility**

# Valuable programs, at global scale



## Technical Deliverables

- Guard against fragmentation
- Manage and progress technical deliverables through work groups and development team
- Administration process and initiation of technical work groups
- Member sandbox portal

## Compliance + Verification

- Develop self serve testing and compliance program
- Develop compliance verification formal service

## Visibility

- Drive constant drumbeat of member and foundation visibility through multiple media
- Engage in industry events and host Foundation events
- Strategic visibility through industry forums, analysts, and media

## Learning + Talent

- Develop multi-level learning modules
- Connections for universities, professors, and course material
- Badge and skill level certification
- Online and event forums for talent matching

## Advocacy + Outreach

- Establish technical advocate program
- Geographic and domain specific advocate-led engagement via formal and informal events and opportunities
- Establish alliances with other organizations

## Marketplace

- Provide online marketplace of providers and products
- Offer RFP matching to members

# Engage!

Drive technical priorities in 20+ focus areas

Opcode Space Mgmt Standing Committee

Software Standing Committee

Base ISA Ratification Task Group

Privileged ISA Spec Task Group

UNIX-Class Platform Spec Task Group

Formal Specification Task Group

Trusted Execution Env Spec Task Group

B Extension (Bit Manipulation) Task Group

J Extension (Dynam. Translated Lang) Task Group

P Extension (Packed-SIMD Inst) Task Group

V Extension (Vector Ops) Task Group

Cryptographic Extension Task Group

Debug Specification Task Group

Fast Interrupts Spec Task Group

Memory Model Spec Task Group

Processor Trace Spec Task Group

Sv128 Specification Task Group

Compliance Task Group

+ Security Committee, HPC Special interest group, and proposed Safety Task Group

Technical Deliverables  
Compliance

# Come together. Right Now.

## Meetups (2,200+ Members)

### Austin Area RISC-V Group

<https://www.meetup.com/Austin-Area-RISC-V-Group/>

### Bay Area RISC-V Group

<https://www.meetup.com/Bay-Area-RISC-V-Meetup/>

### Bristol RISC-V Meetup Group

<https://www.meetup.com/Bristol-RISC-V-Meetup-Group/>

### Cambridge RISC-V Meetup Group

<https://www.meetup.com/Cambridge-RISC-V-Meetup-Group/>

### Israel RISC-V Meetup Group

<https://www.meetup.com/Israel-RISC-V-meetups/>

### Japan RISC-V Association

<https://riscv-association.jp>

### London RISC-V Meetup Group

<https://www.meetup.com/London-RISC-V-Meetup/>

### Osaka

<https://www.fsi-embedded.jp/kumico/column/1596/>

### Pune RISC-V Group

<https://www.meetup.com/Pune-RISC-V-Group/>

### Rocky Mountain Area RISC-V Group

<https://www.meetup.com/Rocky-Mountain-Area-RISC-V-Group/>

### San Diego RISC-V Meetup Group

<https://www.meetup.com/San-Diego-RISC-V-Group/>

### Shanghai RISC-V Meetup Group

<https://www.meetup.com/shanghai-riscv/>

### Seattle RISC-V Meetup Group

<https://www.meetup.com/Seattle-RISC-V-Group>

### Twin Cities RISC-V Meetup Group

<https://www.meetup.com/Twin-Cities-RISC-V-Meetup-Group/>

### Vienna RISC-V Meetup Group

<https://www.meetup.com/Vienna-RISC-V-Meetup/>



Learning + Talent  
Advocacy + Outreach



Develop Education Resources At All Levels



Drive Adoption By Universities



Develop Corporate Education Partnership Programs to Reach Students Globally

# Three membership options to join us



## Premier Member Benefits

- Community level benefits plus...
- Board seat and Technical Steering Committee seat included for \$250k level
- Technical Steering Committee seat included for \$100k level
- Summit speaker session
- Solution provider listing
- 2 case study / blogs per year
- 4 social media spotlights
- Spotlight member profile
- Inclusion in event promotions

## Strategic Member Benefits

- Community level benefits plus...
- Use of RISC-V Trademark for commercialization
- 3 Board reps elected for tier, includes Premier members that do not otherwise have a board seat.
- Eligible to lead workgroup and/or committee
- Solution provider listing
- 1 social media spotlight

## Community Member Benefits

- Accelerated development, reduced risk through open source, ratified ISA.
- Eligible to participate in workgroups, influence strategy and adoption
- 6 support programs in Technical Deliverables, Compliance, Visibility, Learning, Advocacy, and Marketplace
- 1 voting Academic Board rep, 1 non-voting Community Board rep
- Member logo / name listing in website
- Event registration discount

## Premier Requirements

- Membership open to any type of legal entity, not open to individual members
- \$250k Annual membership fee that includes Board seat and TSC seat
- \$100k Annual membership fee that includes TSC seat

## Strategic Member Requirements

- Membership open to any type of legal entity, not open to individual members
- Annual membership fee based on employee size
  - 5,000+ employees \$35k
  - 500-5,000 employees \$15k
  - <500 employees \$5k

## Community Requirements

- Membership open to academic institutions, non-profits, and individuals not representing a legal entity
- No annual membership fee

Note: An organization may not hold more than one seat on the Board or TSC



**Calista Redmond**

CEO, RISC-V Foundation



[www.linkedin.com/company/risc-v-foundation](http://www.linkedin.com/company/risc-v-foundation)

[www.linkedin.com/in/calistaredmond](http://www.linkedin.com/in/calistaredmond)



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[www.riscv.org](http://www.riscv.org)

**Join the  
Revolution**