RISC-V Taiwan Alliance (RVTA) Update

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Taiwan Semiconductor Ecosystem

Highly Specialized Supply Chain

Foundry (Worldwide 70% market share) and OSAT worldwide 50% are both world leading, and IC design 20% next only to the U.S., with extensive IP and design services.

While RVTA gathers industry and academia expertise, momentum of RISC-V is building up primarily by business and research opportunities.

Examples of RISC-V announcements

RISC-V Taiwan Alliance (RVTA)

Foundry

TSMC Open Innovation
Platform (OIP) in
collaboration with
SiFive.

IP

Andes Launches RISC-V FreeStart Program with its Commercial-Grade CPU N22.

Design service

Faraday Unveils RISC-V ASIC Solution to Support Edge AI and IOT SoCs, proven in mass production.

Highlight: Processing in Memory*

Powerchip forms Al Memory Corp. for solutions to the memory wall in computing.

Processing in Memory*

Unprecedented scalable ultra-efficient PIM* architecture and chip

Boosting **20x** data intensive applications

4 Gb DRAM memory chips, embedding 8 processors on die

Power efficiency **10x** better

Delivered as standard DDR4 2400 DIMM modules with 16 chips Source: HOT CHIPS 31, UPMEM 2019 Paper

By reducing drastically CPU-DRAM data movement

Server CPU helped by thousands of additional cores

At marginal cost

RISC-V Application domain from edge to cloud

Andes V5 Adoption

Applications:

- AloT at the edge
- Block chain
- Communication: BT, WiFi, 5G
- Datacenter Al accelerator
- SSD: enterprise/consumer
- Security

- **FPGA**
- MCU
- Multimedia: A/V, AR/VR

50% use Al

40nm to 7nm



Cloud

RISC-V Application domain from edge to cloud

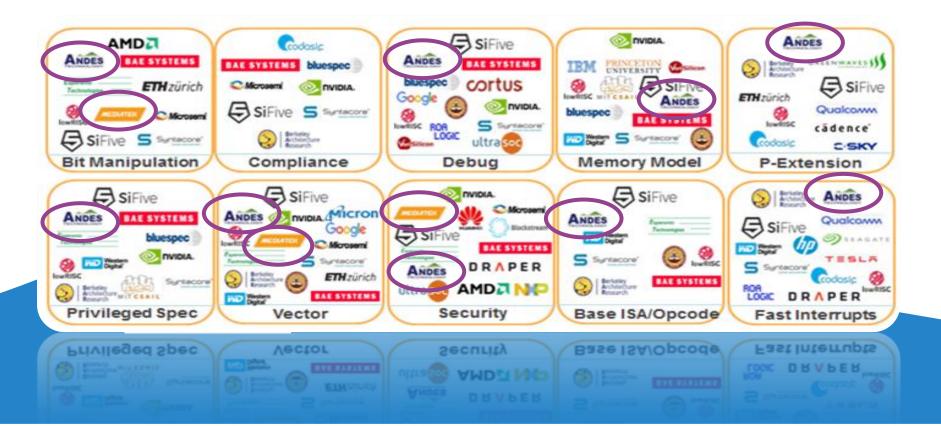
Andes just announced it achieved a record of 125 licensing agreements for its new family of RISC-V processors during the year of 2019 so far.





Contribution in Foundation Task Groups

RISC-V Taiwan Alliance (RVTA)



GNU-Based Toolchains

- binutils, GCC: May, 2017
- glibc: February, 2018
 only supports ryd4i-based ISAs
- · newlib: August, 2017
- · "Probably not a compiler bug"







GNU Toolchains

RISC-V LLVM Porting Effort

- Alex Bradbury is in charge of RISC-V LLV:**M
 - Talk yesterday afternoon
 - Poster on Tuesday night
- RV32IM[A]FD support upstream
 - Missing hard-float calling convention
 - Missing 64-bit support
 - Missing compressed support
- · Clang, Go, and OpenJDK have run code
 - o Rust port in progress
 - Poster on Tuesday



ANDES





SiFive

RISC-V Linux Kernel Port

- Linux: January, 2018
- Only RV64I-based systems
- Drivers are trickling in now







Contribution in software ecosystem















RISC-V in University research is growing

RISC-V Taiwan Alliance (RVTA)

















RISC-V Taiwan Alliance

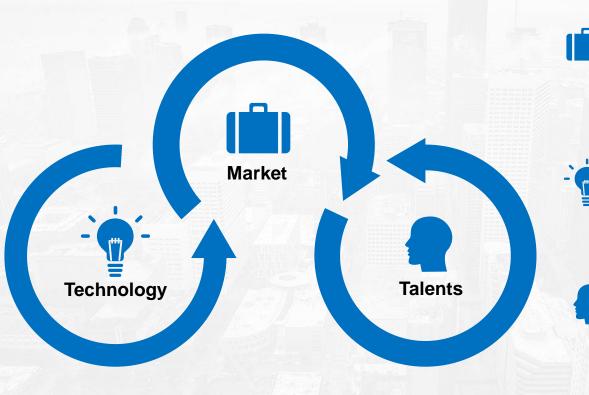
- Established on March 7th, 2019
- Initiated by Taiwan IOT industry association

RISC-V TAIWAN Alliance (RVTA) is committed to coordinating industry, academic, and research institute to work together and introduce RISC-V open architecture to Taiwan.

As soon as we connect resources from RISC-V ecosystems worldwide, Taiwan's R&D, design and application will be capable of integrating AIOT and hitchhiking 5G trends and business opportunities, improving Taiwan's industrial competitiveness.

Mission

RISC-V Taiwan Alliance (RVTA)





Support Taiwan's semiconductor business to enter the core customization of IC design and expedite the RISC-V open architecture into commercial market.



Technology

Promote RISC-V technology and accelerate the development of AloT and edge computing industry in Taiwan.



Talents

Cultivate talents, and connect resources from RISC-V ecosystems worldwide, making Taiwan's ICT industry a key player in the global supply chain and core AloT solution provider.

Our Members

RISC-V Taiwan Alliance (RVTA)

























What we have achieved

- Mar 7th, 2019
 RVTA was established
- May 22nd, 2019
 Chairman Wang visited MIIT in Beijing
- May 29th, 2019
 RVTA hosted the RISC-V forum at COMPUTEX TAIPEI
- Jul 30th & Sep 17th ,2019
 RVTA co-hosted cross-strait
 standards forum in RISC-V
 section



RISC-V Taiwan activities 2020

RISC-V Taiwan Alliance (RVTA)

Event in Trade Show

Embedded
Technology
Design Forum
at COMPUTEX
TAIPEI

June

April —

VLSI-TSA & VLSI-DAT Symposium

Campus promotion

Aug.

VLSI Design/ CAD Symposium

Summer Workshop

Cross-Strait Standards Forum

Discussion in RISC-V open architecture standards

Sep.

Concluding Remarks

RISC-V Taiwan Alliance (RVTA)

Community is a great force to advance technologies.

But, you must be able to work with it and tolerate its pace.





www.twiota.org/risc-v

THANK YOU!